Pentacene organic thin-film transistors on flexible paper and glass substrates



2014 Nanotechnology 25 094005

(http://iopscience.iop.org/0957-4484/25/9/094005)

IOP Publishing Nanotechnology
Nanotechnology **25** (2014) 094005 (7pp) doi:10.1088/0957-4484/25/9/094005

# Pentacene organic thin-film transistors on flexible paper and glass substrates

**Adam T Zocco[1], Han You[1], Joshua A Hagen[2] and Andrew J Steckl[1]**

[1] Nanoelectronics Laboratory, Department of Electrical Engineering and Computing Systems, University of Cincinnati, Cincinnati, OH 45221-0030, USA
[2] US Air Force Research Laboratory, Human Effectiveness Directorate, Wright-Patterson Air Force Base, Dayton, OH 45433, USA

E-mail: a.steckl@uc.edu

Received 25 August 2013, revised 14 October 2013
Published 12 February 2014

**Abstract**
Pentacene-based organic thin-film transistors (OTFTs) were fabricated on several types of flexible substrate: commercial photo paper, ultra-smooth specialty paper and ultra-thin (100 $\mu$M) flexible glass. The transistors were fabricated entirely through dry-step processing. The transconductance and field-effect mobility of OTFTs on photo paper reached values of $\sim$0.52 mS m$^{-1}$ and $\sim$0.1 cm$^2$ V$^{-1}$ s$^{-1}$, respectively. Preliminary results on the lifetime of OTFTs on photo paper yielded stable transconductance and mobility values over a period of more than 250 h. The comparable characteristics of OTFTs fabricated on widely available, low cost paper and high quality expensive liquid crystal display glass indicate the potential importance of cellulose-based electronic devices.

Keywords: OTFT, cellulose, pentacene, paper, thin films

(Some figures may appear in colour only in the online journal)

## 1. Introduction

Organic electronics that use semiconductors consisting of small organic molecules or polymers are finding an increasing range of device applications [1], including organic light emitting diodes (OLEDs), organic photovoltaic (OPV) devices and organic thin-film transistors (OTFTs). Most organic electronics are fabricated on rigid glass substrates. However, in order to take advantage of their flexible nature and low cost roll-to-roll technology, they need to be fabricated on flexible substrates. In this context the development of organic electronics on paper is very attractive as it could be extrapolated to existing high efficiency printing press technology-based products, and has therefore become a prime target for further investigation. Considerable progress is being made in the area of paper electronics [2, 3], with many types of devices being reported. Cellulose-based paper substrates were implemented as an electronic substrate as early as 1969 [4], with most advances occurring in the past decade largely due to technological improvements in thin-film deposition and organic materials [5]. A few notable examples of OTFTs on paper include the report from the Berggren group in 2002 of OTFTs as electrochemical pixels on paper substrates [6]. In 2004, Kim *et al* [7] reported OTFT arrays on paper using poly (3-hexylthiophene) as the semiconductor layer and Eder *et al* [8] reported paper-based ring oscillators. More recently, the Klauk group [9] reported a novel approach to organics on paper by integrating thin-film transistor circuits on banknotes. It should be pointed out that significant development of paper electronics has also occurred using thin-film *inorganic* semiconductors. Several groups have developed oxide-based semiconductor (such as indium gallium zinc oxide, IGZO) TFTs on paper substrates [4, 10–14].

This paper reports on pentacene OTFTs fabricated on paper substrates by an all dry-step process, which uses vacuum evaporation in conjunction with shadow masking techniques. The key advantage of dry processing is a simple patterning technique without the exposure of the substrate to liquids involved in conventional photolithography. Pentacene was selected as the semiconductor layer because it is one of the most widely studied organic semiconductors [15] and therefore serves as a good point of reference. The objective of this study is to compare the performance of pentacene OTFTs on paper substrates with that of devices fabricated

 

by the same dry processes on standard 1 mm thick rigid liquid crystal display (LCD) glass (Corning 1737) and on ultra-thin (100 $\mu$m) flexible glass (Corning Willow$^{TM}$ glass). Two paper materials were investigated as OTFT substrates: 250 $\mu$m thick commercially available photo paper (Hewlett Packard), and 180 $\mu$m thick specialty ultra-smooth paper (Sappi High Gloss). The paper substrates were used as-received without the application of additional protective layers. Excluding the LCD glass, all substrates were highly flexible.

## 2. Experimental details

### *2.1. Methods*

*2.1.1. OTFT fabrication.* Fabrication was carried out on pre-cut LCD ($2'' \times 2''$) and Willow ($1.5'' \times 1''$) glass substrates, along with unmodified cellulose-based photo paper and specialty paper. Test devices were configured in a bottom-up (top-contact) staggered thin-film transistor structure, as shown in figure 1(a). In order to minimize variation caused by substrate flexibility, scissor-cut paper substrates ($1.5'' \times 1.5''$) were fixed to a clean glass substrate with double-sided Kapton$^{TM}$ tape. The copper gate layer ($\sim$145 nm) was radio frequency sputter deposited in a Denton Vacuum system at a base pressure of $1 \times 10^{-6}$ Torr. In the dry-status process used to fabricate the OTFTs, no conventional photolithography was utilized. Instead, patterning of the gate layer was performed through a polyimide shadow mask and the contact pads were masked with a PDMS stamp before the subsequent deposition of the dielectric film. Parylene C (PC) was chosen as the insulator layer for several reasons: it is deposited by a very simple dry process, it has good mechanical flexibility and a dielectric constant ($k > 3$) that is fairly high for vapor-processed polymer dielectrics. PC dimer was vapor deposited in a specialty coatings system PDS 2010 with a thickness of $\sim$340 nm. Capacitance measurements of the PC layer on individual capacitors fabricated on glass showed an average value of 10.2 nF cm$^{-2}$, corresponding to $k \approx 3.9$. As the active organic semiconductor, 47 nm of pentacene (99.995% purity, Sigma Aldrich) was thermally evaporated at a rate of $\sim$ 0.5–0.9 Å s$^{-1}$ directly onto the PC surface through a mechanically milled metallic shadow mask in isolated regions over the gate electrode (see dark regions over the gate electrode in figure 1(b)). The substrate temperature during pentacene deposition was elevated slightly to a stable level in the 31–35 °C range, which is reported to lead to better morphological growth and higher molecular ordering [16, 17]. Finalizing the devices, source and drain patterns were formed by thermal evaporation of 90 nm of gold (99.99%, ESPI) onto the pentacene layer through a second mechanically milled metallic shadow mask. The transistor had device length ($L$) and width ($W$) dimensions of 50 $\mu$m and 500 $\mu$m, respectively. Figure 1(b) shows a completed OTFT array fabricated on specialty paper.

*2.1.2. Electrical properties.* In general, the two key parameters for both inorganic and organic field-effect transistor (FET) operation are the transconductance and the field-effect

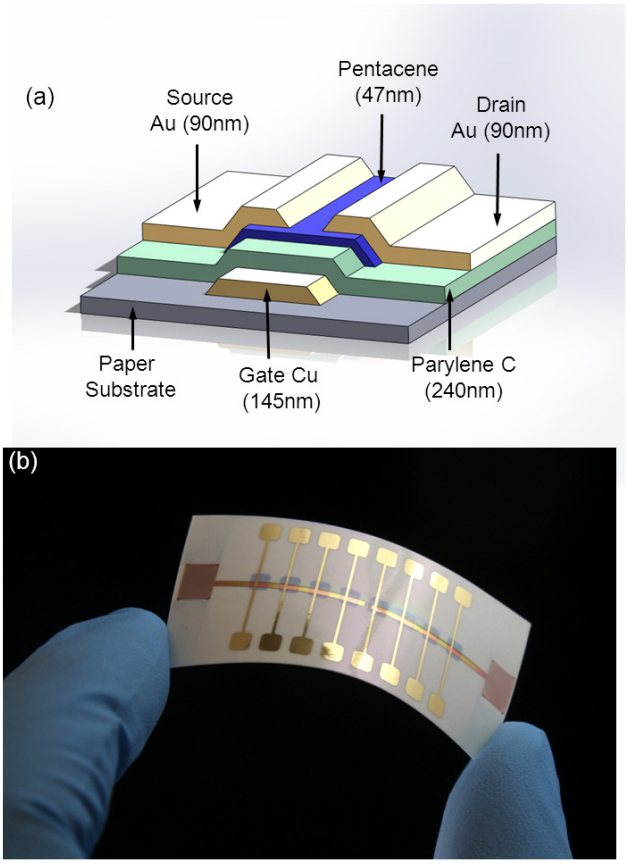


**Figure 1.** Organic thin-film transistors on paper. (a) Staggered bottom-gate (top-contact) device structure: cellulose-based paper substrate, copper gate electrode Parylene C dielectric layer, pentacene semiconductor layer and Au source/drain electrodes. (b) Array of pentacene transistors on a paper substrate fabricated by dry-step processing.

mobility, even if the actual transport mechanisms are different. At low values of drain–source voltage ($V_{DS}$), the FET drain–source current ($I_{DS}$) increases monotonically with $V_{DS}$. This is the linear regime [5, 18]

$$I_{DS,lin} = \frac{\mu_{lin} C_i W}{L}\left(V_{GS} - V_T - \frac{1}{2}V_{DS}\right)V_{DS}, \quad |V_{DS}| < |V_{GS} - V_{th}| \text{ (linear regime)}, \tag{1}$$

where $V_{GS}$ is the gate–source voltage, $V_T$ is the threshold value of $V_{GS}$ for observable $I_{DS}$ flow, $C_i$ is the insulator capacitance per unit area and $W/L$ is the transistor channel aspect ratio. The $I_{DS}$ saturation regime occurs when $V_{DS}$ is larger than $V_{GS}$ minus $V_T$

$$I_{DS,sat} = \frac{\mu_{sat} C_i W}{2L}(V_{GS} - V_T)^2, \quad |V_{DS}| > |V_{GS} - V_{th}| \text{ (saturation regime)}. \tag{2}$$

Here $\mu_{lin}$ and $\mu_{sat}$ are the linear and saturated regime mobilities. Following the notation of Klauk [5] and of Wang and Cheng [18], the transconductance ($g_m$), which describes drain current modulation through change in gate voltage, is given

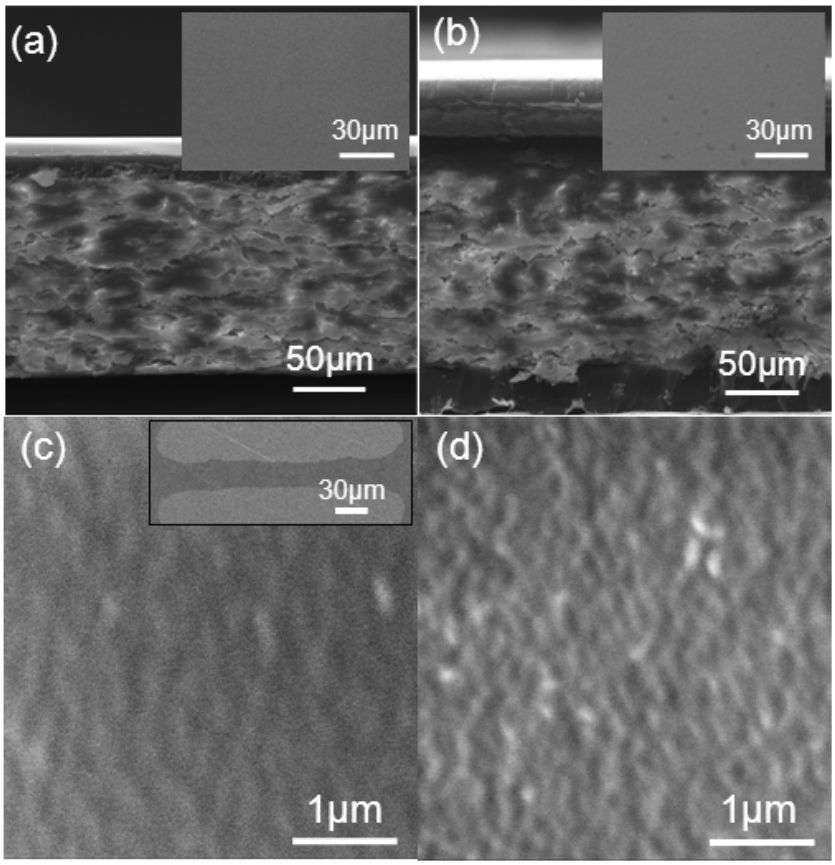


**Figure 2.** SEM microphotographs: (a) specialty paper substrate, cross-section and low magnification top view; (b) photo paper substrate cross-section and low magnification top view; (c) OTFT pentacene layer on specialty paper substrate, high magnification top view (inset, top view of the channel region of the completed OTFT); (d) OTFT pentacene layer on photo paper substrate, high magnification top view.

by

$$g_{\mathrm{m}} = \frac{\partial I_{\mathrm{DS}}}{\partial V_{\mathrm{GS}}}. \tag{3}$$

In the linear and saturation regimes, the transconductance varies linearly with voltage (either $V_{\mathrm{DS}}$ or $V_{\mathrm{GS}}$) and the corresponding value of mobility

$$g_{\mathrm{m,lin}} = \frac{\mu_{\mathrm{lin}} C_{\mathrm{i}} W}{L} V_{\mathrm{DS}}, \quad |V_{\mathrm{DS}}| < |V_{\mathrm{GS}} - V_{\mathrm{th}}| \text{ (linear regime)} \tag{4}$$

$$g_{\mathrm{m,sat}} = \frac{\mu_{\mathrm{sat}} C_{\mathrm{i}} W}{L} (V_{\mathrm{GS}} - V_{\mathrm{T}}), \quad |V_{\mathrm{DS}}| > |V_{\mathrm{GS}} - V_{\mathrm{th}}| > 0 \text{ (saturation regime).} \tag{5}$$

The mobility in the linear and saturation regimes is given by [5]

$$\mu_{\mathrm{lin}} = \frac{L}{C_{\mathrm{i}} V_{\mathrm{DS}} W} \left( \frac{\partial I_{\mathrm{DS}}}{\partial V_{\mathrm{GS}}} \right), \quad |V_{\mathrm{DS}}| < |V_{\mathrm{GS}} - V_{\mathrm{th}}| \text{ (linear regime)} \tag{6}$$

$$\mu_{\mathrm{sat}} = \frac{2L}{C_{\mathrm{i}} W} \left( \frac{\partial \sqrt{I_{\mathrm{DS}}}}{\partial V_{\mathrm{GS}}} \right)^2, \quad |V_{\mathrm{DS}}| > |V_{\mathrm{GS}} - V_{\mathrm{th}}| > 0 \text{ (saturation regime).} \tag{7}$$

The threshold voltage ($V_{\mathrm{T}}$) of the OTFT can be obtained from equation (2) by extrapolating a linear fit to the steepest slope of the $\sqrt{I_{\mathrm{DS}}}$ versus $V_{\mathrm{GS}}$ curve. Finally, another important OTFT characteristic is the ratio of maximum to minimum drain–source current through the device, the so-called on/off ratio.

*2.1.3. Electrical characterization.* Room temperature electrical property measurements were performed with a HP4140B pA meter with custom LabView software and an Alessi 3200 probe station in a semi-dark box in air.

## 3. Results and discussion

One of the key characteristics of the paper substrates is the condition (morphology and roughness, Ra) of the surface on which the OTFTs will be fabricated. Figure 2 shows microscopic images of the specialty paper and photo paper materials using scanning electron microscopy (EVEX). The literature suggests that a smooth starting surface favors suitable pentacene morphological growth, necessary for higher performance in OTFTs [19, 20] mainly due to enhanced molecular ordering and the formation of fewer defect states [21]. Figures 2(a) and (b) show SEM microphotographs of the cross-section of the paper samples. In both cases the cellulose base substrate and

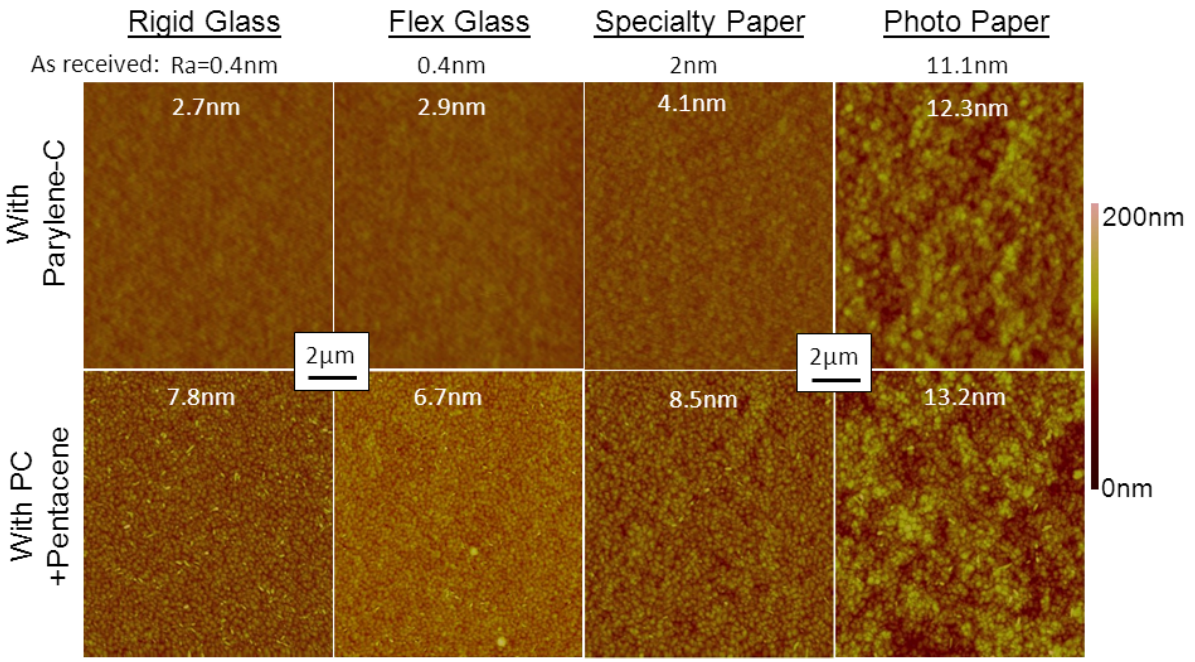


**Figure 3.** AFM scans of thin films deposited on rigid glass, flexible glass, specialty paper and photo paper: parylene C (PC) and pentacene-on-PC. The vertical color bar indicates the range of surface topology; the average rms roughnesses of the starting substrate and after thin-film deposition are also indicated.

a surface coating, which acts as a very effective smoothing layer for the base material, are observed. Insets in figures 2(a) and (b) show the uniform and featureless top surface of the starting paper substrates. Figures 2(c) and (d) show the top surface of the pentacene layer in the channel region of completed transistors fabricated on specialty and photo papers, respectively. The SEM images indicate that the pentacene layers have a relatively smooth surface, free of major height variations.

The morphology of pentacene thin films has been widely studied in order to understand its effect on transistor performance. A study by Bouchoms *et al* [22] verified the presence of two crystalline phases: a thin-film phase and a bulk phase that is triclinic in nature. Device performance is believed to decrease once the film becomes greater than a critical thickness (∼100 nm for room temperature deposition) and enters the bulk phase. Nucleation of the films is also an important aspect, as grain boundaries can be unfavorable to device performance [19]. Conditions, such as deposition rate, temperature, substrate type, outgassing and cleanliness during deposition of pentacene have a strong impact on growth morphology [23]. Based on these considerations, a pentacene deposition rate of ∼0.5–1 Å $s^{-1}$ was selected, along with a total layer thickness of ∼50 nm.

The surface morphology of the PC layer and of the pentacene layer on PC for each substrate is illustrated in figure 3. Also shown are the roughness values Ra of the as-received substrates and the corresponding roughness values with the added layer(s). The first row of images indicates that the deposition of PC increases the surface roughness by ∼1–2 nm compared to the starting substrates. The addition of pentacene films results in a further increase in Ra of 4–5 nm, except in the case of the photo paper substrate where only a ∼1 nm increase is observed (albeit on a larger value of Ra). While these values of surface roughness are significantly larger than that of the starting substrate, they are still quite acceptable for completing the device fabrication through deposition of a source–drain gold contact layer. AFM analysis of the pentacene layer images contained in the second row of figure 3 displays individual crystallites of lateral dimensions ∼100–200 nm.

Current–voltage ($I$–$V$) characteristics are shown in figure 4 for OTFTs fabricated on paper and glass substrates. The $I$–$V$ plots display the drain–source current ($I_{DS}$) versus drain–source voltage ($V_{DS}$) for a series of fixed gate–source voltage ($V_{GS}$) values. In all cases, the OTFT characteristics follow traditional FET behavior, namely a linear regime at small values of $V_{DS}$ (compared to $V_{GS}$; see equation (1)) followed by a saturated regime where $V_{DS}$ is comparable to or larger than $V_{GS}$ (see equation (2)). The $I$–$V$ characteristics indicate comparable saturation drain–source currents at the various gate voltage values for OTFTs on all four substrates. As expected from conventional FET operation, $V_{GS}$ strongly affects the current flow through the OTFT. This is illustrated in the transfer characteristics shown in figure 5(a), where $I_{DS}$ is plotted versus $V_{GS}$ at a fixed $V_{DS}$ value of −55 V for OTFTs on all four substrates. As expected, all transfer characteristics display a sub-threshold regime between the switch-on voltage ($V_{SO}$, the $V_{GS}$ voltage at which current is first observable) and the threshold voltage. The OTFT on flexible glass has a value of $V_{SO}$ nearly equal to zero, while the OTFTs on the other three substrates have values of $V_{SO}$ larger than +15 V. The values of $V_T$ are in the 20–30 V range for all four OTFTs. More accurate $V_T$ values were obtained from $\sqrt{I_{DS}}$ versus $V_{GS}$ curves (not

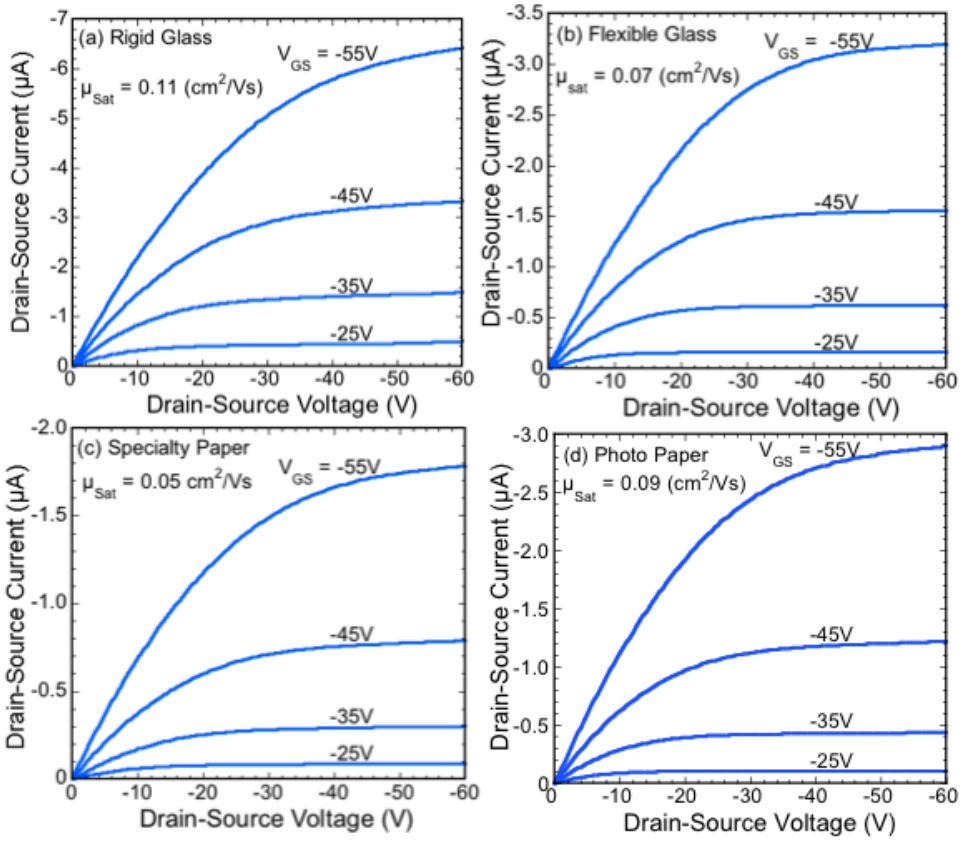


**Figure 4.** Current–voltage operating characteristics of OTFTs on: (a) rigid glass; (b) flexible glass; (c) specialty paper; (d) commercial photo paper.

shown) plotted in the saturation regime (see equation (2)) at $V_{DS} = -55$ V.

The field-effect mobility in the saturation regime was obtained using equation (7). The mobility versus $V_{GS}$ is shown in figure 5(b), at a value of $V_{DS} = -55$ V, for OTFTs on all four substrates. Not unexpectedly, the highest mobility was obtained on the rigid glass substrate, with a value of 0.11 cm$^2$ V$^{-1}$ s$^{-1}$ at $V_{GS} = -55$ V. Interestingly, the OTFT on photo paper exhibits the second highest mobility, with a value of 0.09 cm$^2$ V$^{-1}$ s$^{-1}$. The OTFTs on flexible glass and on specialty paper yield maximum mobility values of 0.07 and 0.05 cm$^2$ V$^{-1}$ s$^{-1}$, respectively.

Table 1 lists the key transistor electrical characteristics of the OTFTs on the four substrates in order of mobility value. The transconductance values in the saturation regime ($V_{DS} = -55$ V) calculated using equation (5) follow the same trend as the mobility, with values of $4.1 \times 10^{-7}$ S (0.82 mS m$^{-1}$) for the OTFT on rigid glass and $2.6 \times 10^{-7}$ S (0.52 mS m$^{-1}$) for the OTFT on the photo paper. The drain current on/off ratio of the OTFTs was measured at $V_{GS} = -55, 0$ V and $V_{DS} = -55$ V. The on/off ratio was strongly affected by the respective sub-threshold currents. The OTFTs on rigid glass and specialty paper, which exhibited significant sub-threshold current, produced on/off ratios of $\sim 1 \times 10^4$. The OTFT on photo paper, which had reduced sub-threshold current, yielded an on/off ratios of $\sim 1 \times 10^5$, while the OTFT on flexible glass which showed the lowest sub-threshold current exhibited the highest on/off ratio of $3 \times 10^6$. For comparison, pentacene OTFTs fabricated on paper by a wet process (photolithography and wet etching) were reported [8] with similar properties, namely a saturated mobility of 0.2 cm$^2$ V$^{-1}$ s$^{-1}$ and an on/off ratio of $\sim 10^6$.

Preliminary lifetime testing of the OTFTs fabricated on photo paper has been carried out. The mobility and transconductance are shown in figure 6 for two different OTFTs as a function of time. The devices were tested in air twice a day, and stored unprotected in a dry nitrogen box. As can be seen in figure 6(b) transistor mobility values remained stable along with the transconductance (figure 6(a)) over a period of $\sim$250 h ($\sim$11 days).

It must be pointed out that the results presented here are obtained from a specific set of devices. While the trends between devices on different substrates are reproducible, parameter values do vary. Therefore, one should interpret these results as indicating that OTFTs fabricated on flexible paper substrates can produce characteristics comparable to OTFTs on conventional and flexible glass.

## 4. Summary and conclusion

In summary, pentacene OTFTs have been fabricated through an all dry-step process on commercial and specialty paper substrates. Comparison devices have been fabricated on rigid

**Table 1.** Electrical properties of OTFTs on the two paper substrates and two glass substrates: saturation mobility and transconductance (both at $V_{DS} = -55$ V); on/off drain current ratio at $V_{GS} = -55, 0$ V, and $V_{DS} = -55$ V.

| Substrate | Mobility ($cm^2\ V^{-1}\ s^{-1}$) | Transconductance (S) | On/off current ratio |
|---|---|---|---|
| Rigid glass | 0.11 | $4.1 \times 10^{-7}$ | $1 \times 10^4$ |
| Photo paper | 0.09 | $2.6 \times 10^{-7}$ | $1 \times 10^5$ |
| Flexible glass | 0.07 | $2.4 \times 10^{-7}$ | $3 \times 10^6$ |
| Specialty paper | 0.05 | $1.5 \times 10^{-7}$ | $1.3 \times 10^4$ |

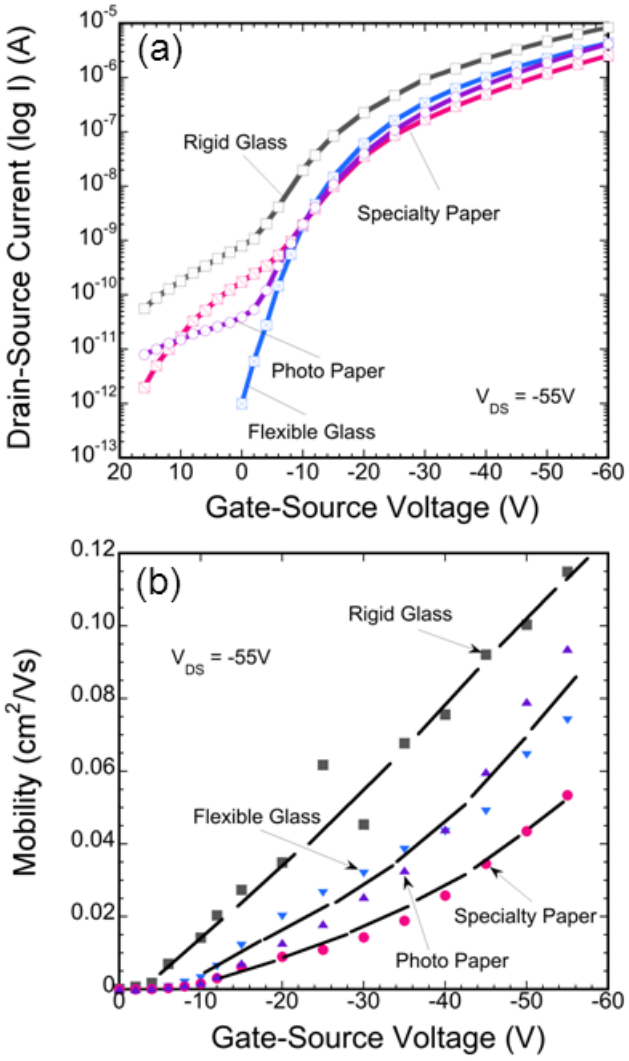


**Figure 5.** Effect of gate–source voltage for OTFTs on several substrates: (a) drain–source current; (b) field-effect mobility.

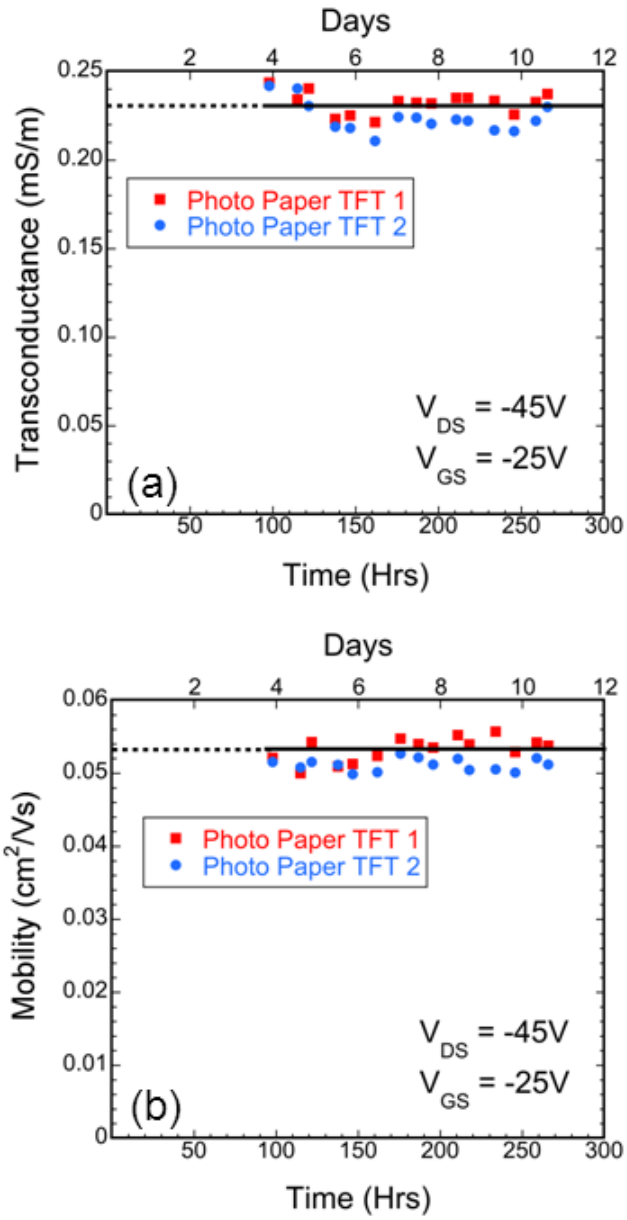


**Figure 6.** Stability of transconductance and mobility of OTFTs on photo paper as a function of time, over a period of 12 days. Measurements performed in air, with storage in a dry box.

and flexible glass substrates. Electrical properties (mobility, transconductance, on/off current ratio) of the OTFT on commercial photo paper are comparable to those on rigid (LCD) glass. Preliminary results on the lifetime of OTFTs on photo paper yielded stable transconductance and mobility values over a period of >250 h. While the mobility of ~0.1 $cm^2\ V^{-1}\ s^{-1}$ obtained for OTFTs on commercial paper is low compared to the best OTFT results obtained with more complex fabrication processes on expensive (glass or Si) substrates, these are encouraging early results. The combination of a low cost commercial paper substrate, a simple dry process and useful electrical characteristics indicate that this represents a promising approach for paper electronics.

## Acknowledgments

Partial support for this research is provided by the US Air Force Research Laboratory. Specialty paper and flexible glass substrates were generously provided by Sappi and Corning, respectively. The authors acknowledge many useful technical discussions with members of the Nanoelectronics Laboratory and the Novel Devices Laboratory at the University of Cincinnati (UC) and the assistance provided by Jeffrey Simkins (UC) in fabricating the shadow masks used in this work.

## References

[1] Forrest F, Burrows P and Thompson M 2000 The dawn of organic electronics *IEEE Spectr.* **37** 29–34
[2] Tobjork D and Osterbacka R 2011 Paper electronics *Adv. Mater.* **23** 1935–61
[3] Steckl A J 2013 Circuits on cellulose *IEEE Spectr.* **50** 48–61
[4] Barquinha P, Martins R, Pereira L and Fortunato E 2012 *Transparent Oxide Electronics: From Materials to Devices* (Chichester, UK: Wiley)
[5] Klauk H 2010 Organic thin-film transistors *Chem. Soc. Rev.* **39** 2643–66
[6] Andersson P, Nilsson D, Svensson P-O, Chen M, Malmström A, Remonen T, Kugler T and Berggren M 2002 Active matrix displays based on all-organic electrochemical smart pixels printed on paper *Adv. Mater.* **14** 1460–4
[7] Kim Y-H, Moon D-G and Han J-I 2004 Organic TFT array on a paper substrate *IEEE Electron Device Lett.* **25** 702–4
[8] Eder F, Klauk H, Halik M, Zschieschang U, Schmid G and Dehm C 2004 Organic electronics on paper *Appl. Phys. Lett.* **84** 2673–5
[9] Zschieschang U, Yamamoto T, Takimiya K, Kuwabara H, Ikeda M, Sekitani T, Someya T and Klauk H 2011 Organic electronics on banknotes *Adv. Mater.* **23** 654–8
[10] Fortunato E, Correia N, Barquinha P, Pereira L, Gonçalves G and Martins R 2008 High-performance flexible hybrid field-effect transistors based on cellulose fiber paper *IEEE Electron Device Lett.* **29** 988–90
[11] Sun J, Jiang J, Lu A and Wan Q 2010 One-volt oxide thin-film transistors on paper *IEEE Trans. Electron Devices* **57** 2258–63
[12] Lim W, Douglas E A, Norton D P, Pearton S J, Ren F, Heo Y-W, Son S Y and Yuh J H 2010 Low-voltage indium gallium zinc oxide thin film transistors on paper substrates *Appl. Phys. Lett.* **96** 053510
[13] Lim W, Kim S H, Norton D P, Pearton S J, Ren F, Shen H and Chang W H 2009 High mobility $InGaZnO_4$ thin-film transistors on paper *Appl. Phys. Lett.* **94** 072103
[14] Martins R, Barquinha P, Pereira L, Correia N, Gonçalves G, Ferreira I and Fortunato E 2008 Write–erase and read paper memory transistor *Appl. Phys. Lett.* **93** 203501
[15] Dimitrakopoulos C D and Malenfant P R L 2002 Organic thin film transistors for large area electronics *Adv. Mater.* **14** 99–117
[16] Horowitz G 1998 Organic field-effect transistors *Adv. Mater.* **10** 365–77
[17] Ling M-M and Bao Z 2004 Thin film deposition, patterning, and printing in OTFTs *Chem. Mater.* **16** 4824–40
[18] Wang Y-W and Cheng H-L 2009 Thickness-dependent threshold voltage in polycrystalline pentacene-based thin-film transistors *Solid-State Electron.* **53** 1107–11
[19] Heringdorf F, Reuter M C and Tromp R M 2001 Growth dynamics of pentacene thin films *Nature* **412** 517–20
[20] Knipp D and Street R A 2004 Pentacene thin film transistors on large area compatible gate dielectrics *J. Non-Cryst. Solids* **338–340** 595–8
[21] Gundlach D J, Lin Y Y, Jackson T N, Nelson S F and Schlom D G 1997 Pentacene organic thin-film transistors—molecular ordering and mobility *IEEE Electron Device Lett.* **18** 87–9
[22] Bouchoms I P M, Schoonveld W A, Vrimoeth J and Klapwik T M 1999 Morphology identification of the thin film phases of vacuum evaporated pentacene on $SiO_2$ substrates *Synth. Met.* **104** 175–8
[23] Choo M H, Kim J H and Im S 2002 Hole transport in amorphous–crystalline-mixed and amorphous pentacene thin-film transistors *Appl. Phys. Lett.* **81** 4640–2