measured profiles is quite good. The residual discrepancies are most likely due to grading effects. Although a few other HJ's showed similarly good fits, for the majority of the devices from the same wafer the discrepancies were about twice as large. On other wafers the discrepancies were larger.

The interface charge density found here is much smaller than the value assumed by Kroemer *et al.*[4] to explain the high photocollection efficiencies of *p-N* HJ's and the absence of rectification for *n-N* HJ's. Devices with such low interface charge should rectify, and we have found that the present HJ's do indeed rectify weakly. The degree of rectification is about what one would expect from the doping and the band structure. The details will be presented elsewhere in a different context.

The conduction band discontinuity found is about 0.07 eV less than the value $0.85\Delta E_g$ one would expect from Dingle's rule.[1] Similar discrepancies were consistently found in all HJ's that exhibited reasonable agreement between measured and reconstructed $\hat{n}(x)$ profiles. By changing the assumed $N_d(x)$, we could have increased ΔE_c by about 0.02 eV, at the expense of an increasing discrepancy between reconstructed and measured $\hat{n}(x)$, but still within acceptable limits. Any larger increase could not be justified.

We speculate that the lower conduction band discontinuities relative to the value of Dingle *et al.*[1] are due to compositional grading. However, care is in order on this matter: our method measures a true electrostatic dipole moment. Such a moment would be present even in a HJ that is so widely graded that the conduction band has become almost flat. A flat conduction band in a widely graded heterojunction does not mean that there is no electrostatic potential difference. It simply means that electrostatic and chemical potential differences cancel each other locally. We would therefore expect our method to yield a finite value for an apparent conduction band discontinuity even for such a widely graded structure, although probably a smaller value than for an abrupt HJ.

We express our appreciation to Steve Wright for many discussions.

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Size effects in $MoSi_2$-gate MOSFET's

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(Received 21 September 1979; accepted for publication 3 December 1979)

Refractory metal silicide gate *n*-channel MOSFET's have been fabricated by rf sputtering from a hot-pressed $MoSi_2$ alloy target. The annealed $MoSi_2$ sheet resistance was 2 $\Omega/\Box$. The MOSFET's were fabricated using plasma etching, projection alignment, and a fully ion-implanted process. Typical values for a 1.7×1.7-μm^2 linear MOSFET are a threshold voltage of 1–1.5 V and a transconductance of 50–100 μmho. Short-channel (length and width) and substrate effects on the threshold voltage are demonstrated.

PACS numbers: 85.30.Tv, 85.30.De

Refractory metal[1,2] and metal silicide[3,4] gate devices are known to be compatible with standard MOS processes, and provide a higher speed capability. While refractory metals have higher conductivity, refractory metal silicides are oxidation resistant and can be used in two-level structures. In this letter, the fabrication and characteristics of short-channel ($<2\,\mu m$) $MoSi_2$-gate MOSFET's are reported.

An integrated-circuit chip was designed containing two matrices of MOSFET's, linear and self-enclosed, with nominal channel dimensions varying from 1.25 to 10 μm in length and from 1.25 to 260 μm in width. A microphotograph of the processed chip is shown in Fig. 1 along with an SEM photograph of a MOSFET with approximately 2 μm channel length. To facilitate automated testing and to minimize external connections, the sources of all MOSFET's, the gates of MOSFET's of equal width, and the drains of MOSFET's of equal length are, respectively, in common.

The devices were made on Czochralski-grown, (100)-oriented, boron-doped, 2–3-Ω cm Si wafers. Field oxide, about 6000 Å thick, was used for device isolation. The field oxide was grown with an isoplanar process. During this step, a composite dielectric of 2000-Å Si_3N_4 and 300-Å SiO_2 was

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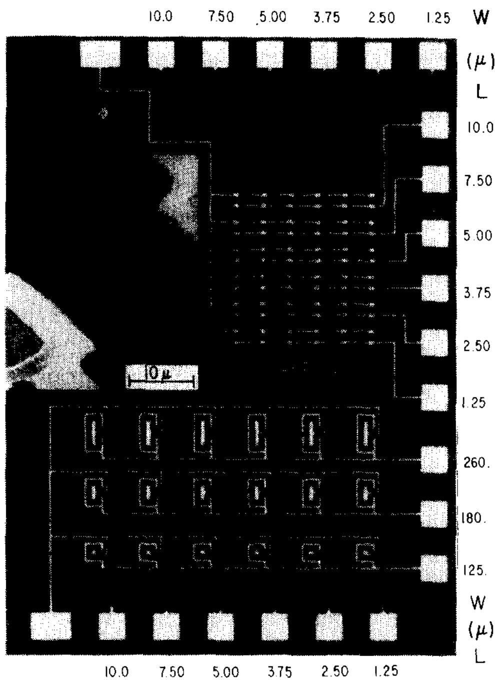


FIG. 1. Microphotograph of the MoSi-gate integrated-circuit chip. The inset is an SEM photograph of a MOSFET with approximately 2 μm channel length. Tilt angle is 50°.

used to protect the future gate region. The thickness of the nitride and oxide was chosen to minimize lateral underoxidation. A field threshold implant was performed with a boron dose of 4×10^{13} ions/cm^2 and energy of 55 keV. The gate dielectric was composed of 300 Å of dry SiO_2 and 300 Å of CVD Si_3N_4. A gate threshold control implant was done with boron at a dose of 10^{12} ions/cm^2 and energy of 40 keV. The nitride layer was used to ensure high yield and device stability. $MoSi_2$ was rf sputtered from a hot-pressed alloy target of stoichiometric composition. Auger electron spectroscopy was used to verify that the film composition was approximately that of $MoSi_2$, namely, Si/Mo ratio of ~ 2.2. The as-deposited $MoSi_2$ had a sheet resistance of 25 $\Omega/\square$ for a 3000-Å film. After a 60-min anneal in hydrogen at 1000 °C, the sheet resistance reached a minimum of 2 $\Omega/\square$. Using x-ray diffraction, it was determined that the as-deposited $MoSi_2$ was amorphous. After the hydrogen anneal the film became

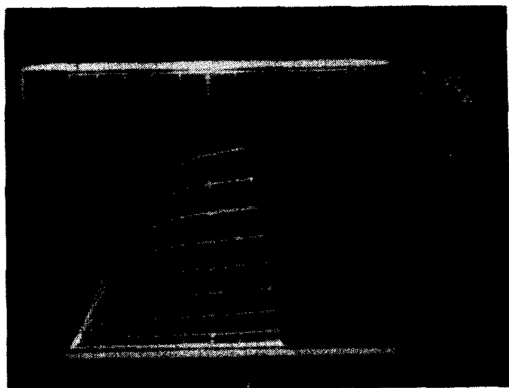
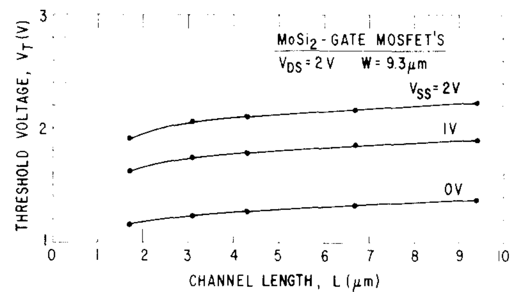
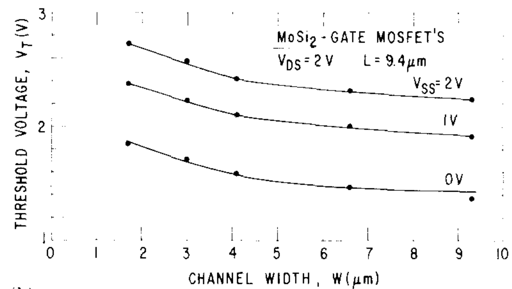
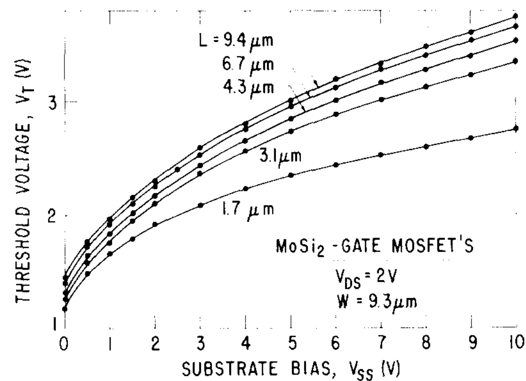


FIG. 2. I-V characteristics of a 1.7×1.7-μm^2 $MoSi_2$-gate linear MOSFET.







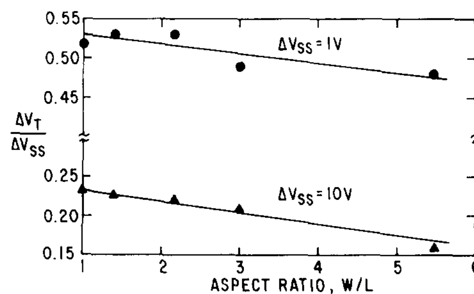


FIG. 3. Threshold voltage of $MoSi_2$-gate MOSFET's as a function of (a) channel length, (b) channel width for $V_{SS} = 0$, 1, and 2 V, and (c) source-to-substrate bias for various channel lengths. (d) $\Delta V_T / \Delta V_{SS}$ as a function of aspect ratio of these $MoSi_2$-gate devices.

polycrystalline with a grain size in the range of 1000 Å. Pattern definition was achieved with a CF_4/4 % O_2 gas plasma at 75 °C. Throughout the process, a 1 : 1 Perkin–Elmer projection aligner and positive photoresist were used for pattern definition. An oxide layer was grown over the $MoSi_2$ in an oxygen ambient at 1000 °C for 1 h. The O/Si ratio in the oxide layer was estimated from Auger analysis to be 2.1. An

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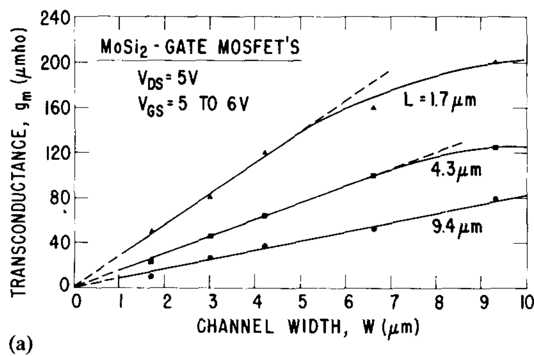
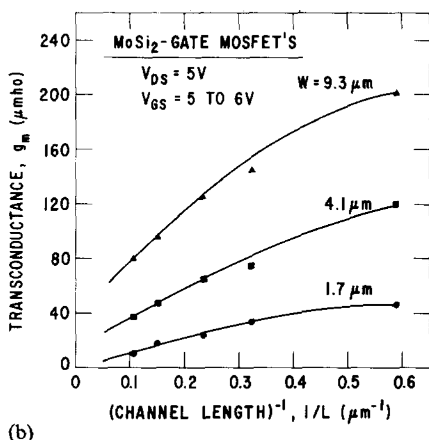


(a)



(b)

FIG. 4. Transconductance g_m of $MoSi_2$-gate MOSFET's as a function of (a) channel width and (b) inverse channel length.

As source-drain implant was performed at a dose of 2×10^{15} ions/cm^2 and an energy of 140 keV. This implant was done through a 300-Å oxide which was then removed and subsequently regrown. A pyrolytically deposited SiO_2 layer of 3000 Å was next deposited and contact vias were opened. Aluminum/2% Si was evaporated for Ohmic contacts to avoid Al spiking through the junction. Most of the process steps, particularly oxide thicknesses and ion implantation doses, were computer simulated using the SUPREM program.[5]

Both linear and self-enclosed $MoSi_2$-gate MOSFET's were operational with low leakage current and desired threshold voltage. The I-V characteristics of the smallest MOSFET fabricated, 1.7×1.7-μm^2 channel, are shown in Fig. 2.

Size effects on threshold voltage are observed for both channel length and width dimensions as shown in Figs. 3(a) and 3(b), respectively. The MOSFET threshold was taken to be the gate voltage at which $I_{DS} = 1\ \mu$A. Short-channel effects are observed for dimensions smaller than 4 μm, resulting in a decreasing V_T with L, and an increasing V_T with W. A strong effect of the substrate voltage, V_{SS}, on V_T was observed for all channel lengths, as shown in Fig. 3(c). The relative substrate voltage effect, $\Delta V_T / \Delta V_{SS}$, is plotted in Fig. 3(d) as a function of MOSFET aspect ratio, W/L, for two V_{SS} increments, 0–1 and 0–10 V. As can be seen, the relative substrate effect is considerably stronger at lower values of ΔV_{SS}.

The transconductance g_m of the $MoSi_2$-gate devices is systematically plotted in Figs. 4(a) and 4(b) as a function of channel width and inverse channel length, respectively. As expected, increasing either the channel width or the inverse channel length results in a higher g_m.

Typically, a 1.7×1.7-μm^2 linear MOSFET has a threshold of 1 to 1.5 V at $V_{DS} = 2$ V and $V_{SS} = 0$ V and $g_m = 50$–$100\ \mu$mho at $V_{GS} = 5$–6 V. The effective channel mobility calculated from these values corresponds to $\mu_{eff} = 150$–300 cm^2/V sec. For a high-W/L ($260\ \mu$m/$1.7\ \mu$m)-ratio self-enclosed MOSFET, a $g_m = 6$ mmho was obtained.

In conclusion, size effects in $MoSi_2$-gate MOSFET's have been investigated. Short-channel effects were observed for W and $L < 4\ \mu$m. Short-channel ($L < 2\ \mu$m) MOSFET operation using this refractory metal silicide gate material was demonstrated.

The authors would like to thank D.M. Brown, M. Ghezzo, and M.E. Motamedi for helpful discussions, G. Smith for performing some of the characterization, and F. Bacon for Auger electron spectroscopy. One of the authors (AJS) also wishes to acknowledge the National Science Foundation for its partial support of this work under Grant ENG78-08422.

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