CMOS-Based Photoreceiver Arrays for Page-Oriented Optical Storage Access

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***Abstract*—In this letter, we report the design, characterization, and page-oriented read demonstration of a 5 × 5 photoreceiver array fabricated within the technology constraints of a standard 1.2-μm CMOS fabrication process. These monolithic circuits include a silicon-based photodetector, a multistage current amplifier, and a thresholding circuit that allows the photoreceiver sensitivity to be tuned over a wide range of optical power levels. In addition to characterizing the performance of individual photoreceiver circuits, we demonstrate the ability to interface directly with very large scale integration logic circuits. Finally, a 5 × 5 photoreceiver array is used to detect and then display a two-dimensional pattern of bits arranged in a page-oriented data format.**

***Index Terms*—CMOS photoreceivers, optical storage interfaces, silicon photodetectors, smart pixel devices.**

I. Introduction

OVER THE NEXT decade, optical storage requirements are expected to reach the terabyte level for personal users and the petabyte level for database and knowledge base applications [1]. While considerable effort has been devoted toward the development of optical storage media capable of meeting this need, relatively little work has been done to develop the optical read head technology that will be necessary to interface these ultra-high-density storage devices with existing electronic computing hardware.

One problem that has been partially addressed is the Von Neumann bottleneck (i.e., data transfer rates in a large-capacity memory system are limited by the bit serial methods used to access the memory). To limitations associated with bit serial data access, it has been suggested that future optical storage systems will provide page-oriented memory access. In particular, the optical storage community has focused on the ability of next generation optical storage media to produce page-oriented optical output.

While the ability to produce page-oriented output may be a necessary feature in large capacity and high data rate optical storage media, the development of a practical optical storage system also depends on the demonstration of optical read head technologies that are capable of reading and processing data in a page-oriented fashion.

Several issues impact the development of read head devices for page-oriented optical storage systems. First, the detector/receiver technology used must be compact and suitable for integration into relatively large two-dimensional (2-D) arrays. Ultimately, the chip area required to implement a photoreceiver circuit will limit the size of the page and thus the aggregate read rate achievable with the read head device. Second, the word-oriented bus architecture of conventional computers suggests that the read head device will require data queues and/or data filtering circuitry. To provide compatibility with this circuitry, the photoreceiver device technology should be compatible with conventional electronic logic circuitry. Ideally, the photoreceiver should be implemented in a CMOS technology that can be fabricated with current device fabrication technologies and directly integrated with existing computer hardware.

Finally, because of the low optical power levels output from page-oriented optical storage media, photoreceivers for page-oriented read heads must be sensitive to extremely low optical power (on the order of a few nanowatts). Although ongoing materials research is likely to increase the output power from each individual bit location, the multibit nature of page-oriented optical storage media suggests that output power per bit will always be reduced by a factor proportional to the page size. Thus, photoreceivers for page-oriented read head devices will always require lower power thresholds than their bit serial counterparts.

A variety of photodetector/photoreceiver technologies has been utilized in the design of smart-pixel-based photonic information processing systems which have many of the same area and technology compatibility issues [2]–[4]. Of particular interest are circuits that monolithically integrate silicon photodetectors with CMOS-based photoreceiver circuitry [5]. In addition to providing compatibility with conventional CMOS logic circuitry, these photoreceiver circuits can be fabricated with existing fabrication technology.

While CMOS-based photoreceivers for smart pixel applications have been shown to provide both high data rates and low bit error rates [6], the minimum optical power requirements for many smart pixel systems is significantly higher than those expected for page-oriented optical storage systems. In fact, implicit in the demonstration of high data rates (up to 1 Gbit/s) and low bit error rate (down to 10^{-10}) is the fact that these performance metrics are only achieved at input power levels orders of magnitude larger than the output power from page-oriented

Manuscript received February 1, 2000; revised May 19, 2000. This work was supported in part by the National Science Foundation under Grant ECS-9813588 and Grant ECS-9906984.

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Publisher Item Identifier S 1041-1135(00)07442-5.

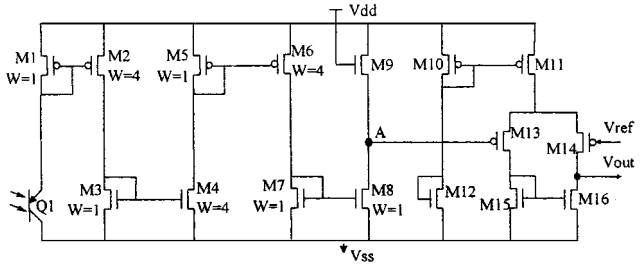

Fig. 1. Circuit diagram of the photoreceiver module.

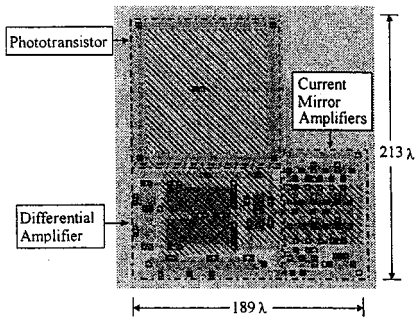

Fig. 2. Layout of the photoreceiver module ($\lambda = 0.6\ \mu$m).

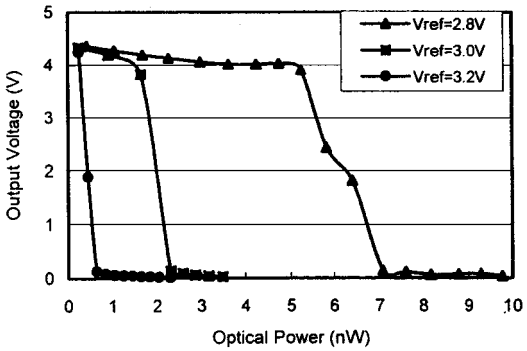

Fig. 3. Output voltage versus incident optical power for a typical photoreceiver circuit.

optical storage media. This tradeoff between sensitivity and data rate presents significant challenges to the design of photoreceiver circuits for application in page-oriented optical storage read heads.

In this letter, we report on the design, characterization, and page-oriented read demonstration of a 5×5 photoreceiver array fabricated within the technology constraints of a standard 1.2-μm CMOS fabrication process available through the MOSIS CMOS foundry service.[1] The photoreceiver incorporates high-gain amplifiers and thresholding circuitry to provide optical power sensitivity that can be tuned over a wide range of optical power levels. In addition to characterizing the performance of individual photoreceiver circuits, the ability to interface directly with very large scale integration (VLSI) logic circuits is demonstrated.

II. Photoreceiver Array Design

As shown in Fig. 1, the demonstrated photoreceiver circuit consists of a bipolar junction phototransistor, a three-stage current amplification circuit, an active load transistor, and an adjustable reference comparator circuit that provides a digital logic output level based on a user defined reference voltage. The phototransistor is implemented using a p^+ diffusion in an n-well to form the emitter and base regions. The p-type substrate (which is grounded in the n-well CMOS process) acts as the lightly doped collector region.

The $60 \times 60\ \mu m^2$ phototransistor ($Q1$ in Fig. 1) is biased in a floating base configuration. In this configuration, transistor action in the device amplifies the photogenerated current, which acts as a base current in the transistor structure. With a weak optical input ($\sim$0.5 nW), $Q1$ produces a current of $\sim$10 nA. This photocurrent is amplified by a factor of 64 gain in the cascade of three current mirrors (transistors $M1$–$M6$) leading to an optoelectronic gain of approximately 1280 A/W.

After cascading through three current gain stages, the amplified current is mirrored through a unity gain NMOS mirror (transistors $M7$ and $M8$) and then dropped across an active load device (transistor $M9$ in Fig. 1) yielding a voltage level that is dropped from the 5-V V_{dd} supply. Thus, as the optical input power incident on the phototransistor is increased, the voltage level at node $\boldsymbol{A}$ in Fig. 1 decreases from 5 V. Notice that this circuit configuration leads to a logical inversion of the optical input signal.

[1]For more information on the MOSIS CMOS fabrication service, see the MOSIS Web page at www.mosis.org

The output stage of the photoreceiver circuit is an adjustable threshold comparator circuit (transistors $M10$–$M16$). The voltage level generated at node $\boldsymbol{A}$ provides one input of the comparator. The other input is a user defined reference voltage provided from off chip. The comparator produces a logic level output based on a comparison between the optically controlled voltage level at node $\boldsymbol{A}$ and the user supplied reference voltage. When the optically controlled voltage is less than the reference voltage (i.e., when the optical input power is above a threshold level), the photoreceiver output goes to logic "0." By varying the reference voltage, the optical power threshold changes.

Fig. 2 shows the CMOS layout for the photoreceiver circuit shown in Fig. 1. This layout has been replicated 25 times on the test chip to form a 5×5 array of photoreceivers. The chips were fabricated using a 1.2-μm CMOS process through the MOSIS foundry service on a 2 mm $\times$ 2 mm "tiny chip" with a 40-pin analog pad frame. As shown in Fig. 2, each photoreceiver circuit fills a 128 μm by 113 μm footprint that includes a 60 μm $\times$ 60 μm photodetector window. It should be noted that with this layout, a 100×100 element array could easily fit on a 1.5 cm $\times$ 1.5 cm CMOS chip. By scaling the layout down to a 0.25-μm gate length technology, a 100×100 element array could be scaled to fit on a 3 mm $\times$ 3 mm CMOS chip.

III. Photoreceiver Performance

An 835-nm diode laser was used to test the photoreceivers. The laser output was split into two beams with a pellicle beam splitter providing a 92/8 splitting ratio. The low-power beam

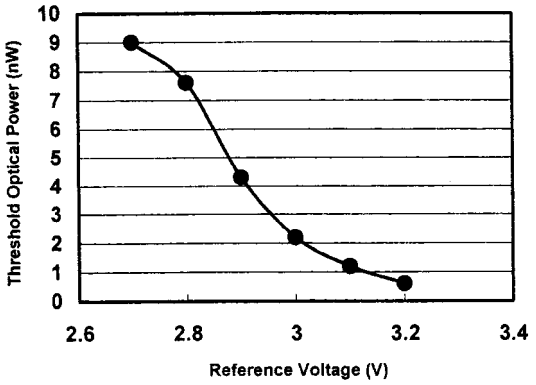

Fig. 4. Optical threshold power versus reference voltage for a typical photoreceiver circuit.

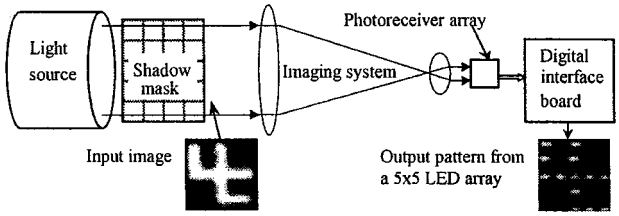

Fig. 5. Optical system and captured input/output images for simulation of a page-oriented read operation using a shadow mask, the 5 × 5 photoreceiver array, a VLSI logic circuit, and a 5 × 5 LED array.

was coupled into a single-mode fiber and aligned to a photodetector window with a three-axes fiber positioner. Photoreceiver input/output characteristics were taken by monitoring the high-power beam with an optical power meter.

Fig. 3 shows a typical output voltage versus incident optical power for different reference voltages. As expected, increasing the reference voltage decreases the optical power threshold (defined as the optical power required to drop the output voltage to 10% of its maximum value). Fig. 4 shows the relationship between optical threshold power and reference voltage for the highly sensitive region of the photoreceiver characteristics. For a reference voltage of 3.2 V, the optical threshold power was ∼0.5 nW (−63 dBm).

To simulate the read operation from a page-oriented memory device, we imaged a shadow mask pattern onto a packaged 5 × 5 photoreceiver array. The photoreceiver array was then used to drive a custom digital interface board comprised of inverters, latches, and line drivers. A 5 × 5 LED array was driven with the line drivers and used to display the output pattern generated by the photoreceiver array. As shown in Fig. 5, illuminated bit positions in the input pattern correspond to bright pixels in the output image.

Our primary objective has been to demonstrate a CMOS-based photoreceiver with sufficient optoelectronic gain to read data from a page-oriented optical storage media. While we have not worked to optimize the frequency response of our photoreceiver circuit, some comments can be made regarding the expected frequency response. First, when used in a floating base configuration, phototransistors have a notoriously slow turn off. To improve the frequency response beyond our measurement of 1 KHz, it would be necessary to replace the phototransistor with a pn junction photodetector similar to those previously reported [6].

Assuming that a fast detector were used, simulation results show that at the maximum sensitivity and minimum detectable light power levels, the frequency response of our receiver circuit would be ∼300 kHz. This frequency is dominated by the response of the current mirrors. It should be noted that the frequency response can be significantly improved by driving the receiver with an optical signal significantly larger than the power threshold. For example if the reference voltage is set for maximum sensitivity and the input power is increased by a factor of ten over the threshold power, then the simulated frequency response improves to provide nearly megahertz operation.

IV. Conclusion

In this letter, we have demonstrated and characterized a photoreceiver technology suitable for accessing page-oriented optical storage media. The photoreceiver circuits were implemented using a conventional CMOS fabrication process that incorporates a photodetector, a multistage current amplification circuit, and a user controlled comparator circuit. Individual photoreceivers were shown to have minimum threshold powers less than 1 nW. To demonstrate page-oriented reading and compatibility with existing electronics, a 5×5 array of photoreceivers was connected to a digital interface board that included inverters, latches, line drivers and a 5 × 5 LED array. When the photoreceiver array was illuminated through a shadow mask, the detected bit pattern was reproduced by the LED array on the interface board.

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