High-Voltage Ni– and Pt–SiC Schottky Diodes Utilizing Metal Field Plate Termination

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***Abstract*—We have fabricated 1 kV 4H and 6H SiC Schottky diodes utilizing a metal-oxide overlap structure for electric field termination. This simple structure when used with a high barrier height metal such as Ni has consistently given us good yield of Schottky diodes with breakdown voltages in excess of 60% of the theoretically calculated value. This paper presents the design considerations, the fabrication procedure, and characterization results for these 1 kV Ni–SiC Schottky diodes. Comparison to similarly fabricated Pt–SiC Schottky diodes is reported. The Ni–SiC ohmic contact formation has been studied using Auger electron spectroscopy and X-ray diffraction. The characterization study includes measurements of current–voltage ($I-V$) temperature and capacitance–voltage ($C-V$) temperature characteristics. The high-temperature performance of these diodes has also been investigated. The diodes show good rectifying behavior with ON/OFF current ratios, ranging from 10^6 to 10^7 at 27 °C and in excess of 10^6 up to 300 °C.**

***Index Terms*—Power devices, Schottky diodes, silicon carbide.**

I. Introduction

SiC is receiving increased attention as a semiconductor material for high-power, high-temperature, and high-frequency devices for applications in aerospace and ground-based power systems. Recent comprehensive reviews of the status of SiC materials and device technology can be found in [1] and [2]. Devices based on SiC can offer fast switching characteristics and high-power handling capability often needed for such applications. Due to the higher breakdown electric field and wider band gap of SiC, high-voltage (>200 V) Schottky diodes with relatively lower leakage current and on-resistance compared to Si Schottky diodes can be fabricated on SiC. These Schottky diodes have the potential to be a valuable alternative to Si-based switching devices for applications where both power and speed need to be delivered.

For high-voltage Schottky diodes, it is necessary to have an edge termination around the periphery of the diodes to reduce the electric field crowding at the diode edges. The experimentally obtained values of breakdown voltage for SiC Schottky diodes without edge termination have been found to be considerably lower than those with some form of edge termination. Several techniques have been shown to reduce the field crowding at the edges, thus resulting in higher breakdown voltages. These include 1) the use of floating metal field rings (FMR) and resistive Schottky barrier field plates (RESP) as reported by Bhatnagar *et al*. [3]; 2) the use of implantation of neutral species at the periphery of the diode to form an amorphous area around the periphery of the device [4]–[7]; and 3) the p-n junction guard-ring termination formed by a local oxide process (LOCOS) [8]. In most of these structures, the SiC surface is unpassivated and there is no dielectric isolation between devices on the chip.

At Cincinnati, we have developed a simple metal field plate structure in which the Schottky contact overlaps a thermally grown SiO_2 layer so that the maximum electric field at any applied bias ($E_{\max}$) is at the SiO_2-metal interface. The lateral metal overlap on the oxide layer is approximately equal to the thickness of the SiC epi-layer. For such a structure, the breakdown voltage should ideally not be affected by electric field crowding. In addition, the oxide layer grown serves two other purposes 1) surface passivation; and 2) removal of surface defects from the SiC layer which upon oxidation is etched off from the areas where the Schottky contact is to be formed. We first reported this structure for fabricating high-voltage SiC Schottky diodes in 1993 [9], [10], and since then we have consistently achieved good results with this approach [11]–[15]. We were also the first to utilize Ni for both Schottky and ohmic contact due to its refractory nature (allowing high-temperature operation), and large barrier height to 3C–SiC [9], [10], 6H–SiC [11]–[13], and 4H–SiC [14], [15]. The use of metals such as Ni that form a large barrier height on SiC allow operation of diodes at higher temperature with lower power losses compared to metals such as Ti which have relatively smaller barrier height to SiC, as discussed later. Since our first reports, several other groups have adopted the metal overlap structure using Ni for both Schottky and ohmic contact to achieve high voltage breakdown on SiC [16], [17].

II. Theoretical Considerations

The barrier height of the metal-Schottky contact plays a critical role in the leakage current and the on-state voltage drop of the Schottky diodes. Selection of the metal to be used for the Schottky contact is thus based on the power losses of the diode which are dependent on the temperature at which the diode is to be operated. In forward bias, since the on-resistance

Manuscript received September 21, 1998; revised October 12, 1998. This work was supported by grants from the Ohio Aerospace Institute and Wright-Patterson Air Force Base. The review of this paper was arranged by Editor D. Stephani.

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Publisher Item Identifier S 0018-9383(99)01691-3.

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of SiC Schottky diodes is low, the dominant component of the voltage drop occurs across the metal-SiC Schottky barrier. Thus diodes utilizing metals with a larger Schottky barrier to SiC have larger on-state voltage drop. However, for high-temperature operation of SiC power rectifiers, such metals are still preferable because they also result in lower leakage currents. In other words, the overall ON/OFF ratio of the Schottky diode is higher if we use metals that form a larger Schottky barrier.

To determine the optimum barrier height of the Schottky contact, the static power-loss analysis can be performed for rectifiers operating at a 50% duty cycle. Under these conditions, the maximum sum of static power loss (P_L) dissipated during the on-state and the off-state per unit area is given by (1), provided that the reverse current density follows theoretical considerations [18]

$$P_L = \frac{1}{2}(J_F V_F + J_R V_R). \tag{1}$$

The calculated power losses for 1 kV SiC Schottky diodes as a function of metal barrier height and temperature show [18] that it is more efficient to use metals that form large barrier heights ($\geq$1.2 eV) if operation of diodes at higher temperatures is desired. Our objective was to operate the diodes at high temperatures (at least 300 °C) and our preliminary studies [9], [10] as well as reports from other researchers [19] had shown that Ni results in suitably large barrier heights (1.2–1.3 eV) to SiC. Thus, we have utilized this metal extensively to study high-voltage Schottky rectifiers on 4H– and 6H–SiC for high-temperature applications.

III. Fabrication Procedure

SiC wafers with a 10-μm thick lightly doped (mid 10^{15}–10^{16} cm^{-3}) n-type epi-layer grown on highly doped (10^{18}–10^{19} cm^{-3}) n-type Si-face 6H– or 4H–SiC substrate commercially available from Cree Research [20] were utilized to fabricate Schottky diodes. Fig. 1 shows the schematic of the metal overlap structure utilized. A 550 Å thermally grown oxide on the epi-layer served both as a passivation layer for regions away from the Schottky contact and as a sacrificial layer for regions where contacts were formed. The oxidation was performed under wet O_2 ambient at 1150 °C for 5 h and was followed by a 30 min anneal in Ar ambient. An additional 2500 Å layer of SiO_2 was deposited by sputtering. After oxidation, a backside ohmic contact was formed by Ni sputter deposition followed by a 5-min. rapid thermal annealing in Ar ambient at 950 °C. The wafer temperature during Ni ohmic contact metal deposition was held at 200 °C, and the chamber pressure was 6 mTorr. These deposition conditions resulted in low resistivity (<10 $\mu\Omega$-cm) Ni films. Prior to the Schottky metal deposition, the sacrificial oxide layer in the regions where contacts are to be formed was patterned and removed by etching in buffered HF solution. The Schottky contacts thus formed had a circular geometry, with diameters varying from 30 to 240 μm. The contacts were designed with the metal overlapping the field oxide by 10 μm to improve field termination at the edges. For comparison to the Ni diodes, we have fabricated several diodes using Pt,

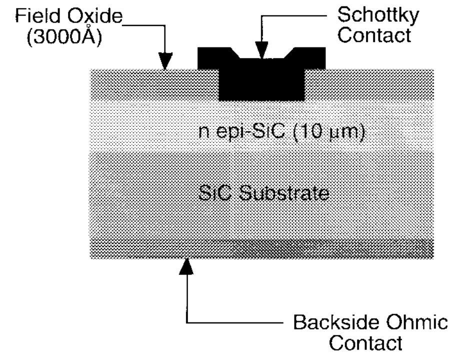


Fig. 1. Schematic of the SiC Schottky diode structure, showing the field oxide, the overlapping metal electrode, and the epi-layer drift region.

which has a lower Schottky barrier to SiC. Sputter-deposition was utilized to deposit metal (Ni or Pt) for the Schottky metal contact. The temperature of the wafers was held at 175 °C for Ni deposition, and 200 °C for Pt deposition. Standard lithographic process and wet chemical etching (in diluted aqua-regia) was utilized to pattern the Schottky contacts. Finally, Au wire bonding was utilized to make connections from the devices to a package which consisted of a gold-plated metal frame wrapped in ceramic. Fig. 2(a) shows an array of 1 kV Schottky diodes on a SiC chip fabricated following this procedure, while Fig. 2(b) shows a packaged SiC chip.

IV. Results and Discussion

A. Ohmic Contact Formation and Interface Analysis

The nature and characteristics of the Ni contact on SiC is determined by the thermal treatment of the deposited film. We have found in our studies that as-deposited Ni film forms a Schottky contact which remains stable at temperatures up to 600 °C. At temperatures higher than 600 °C, we have found evidence of Ni–silicide formation in Ni/SiC samples, as shown in the Auger electron spectroscopy (AES) depth profiles of Fig. 3, and in the X-ray diffraction (XRD) spectra of Fig. 4. The AES profiles indicate that the Ni/6H–SiC interface after a 600 °C thermal annealing [Fig. 3(b)] remains identical to that without annealing [Fig. 3(a)]. However, after annealing at 900 °C, the interaction between Ni and SiC is evident, as indicated in Fig. 3(c). Similar observations have been obtained by XRD, as shown in Fig. 4. Ni–silicides, detected by XRD performed on Ni/6H–SiC samples after 900 °C annealing, are believed to be the reason for ohmic contact formation. It is also observed from the Auger depth profile that carbon atoms released from SiC due to the formation of Ni–silicides under high-temperature annealing, have accumulated within the SiC interface region or incorporated into the Ni–silicide region. The existence of these carbon-rich regions, though still not clear in effect, may be one reason for the higher contact resistance observed in Ni–SiC ohmic contacts. To eliminate carbon "contamination," new approaches may be required in future studies.

Formation of Ni–silicide as evidenced from the above interface analysis reduces the contact resistance for Ni/SiC ohmic contacts as the anneal temperature is increased up to

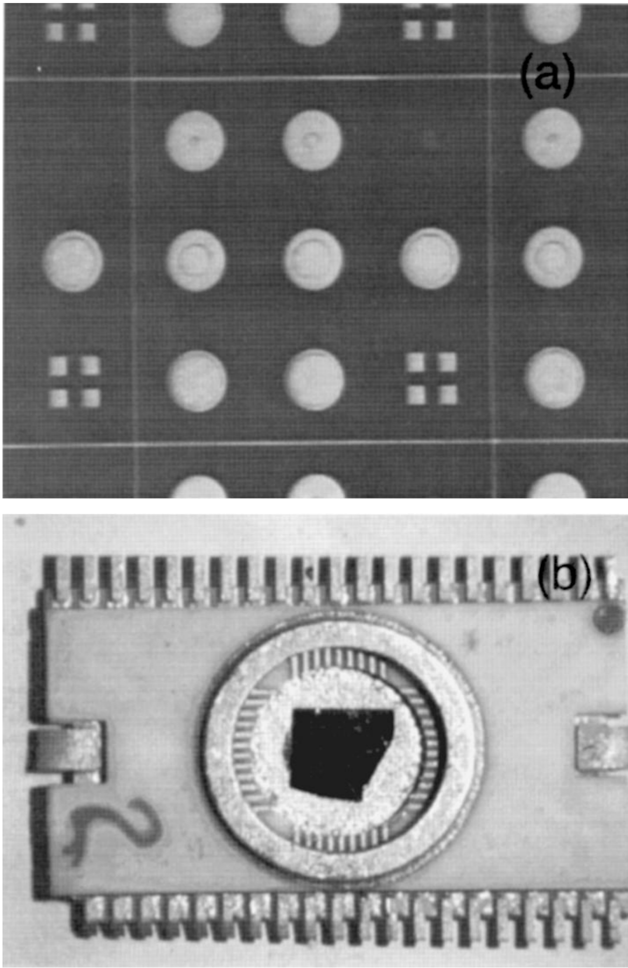


Fig. 2. Fabricated 1 kV Ni/6H–SiC Schottky diodes: (a) array of diodes of different sizes on a SiC chip and (b) packaged SiC chip.

900 °C. The specific contact resistance was measured using the circular transmission line method (CTLM). The $I-V$ curves were measured between a large contact area and the individual dots which are separated by isolation rings. It was observed that increasing the anneal temperature beyond 950 °C did not reduce the contact resistance any further. The specific contact resistivity after 950 °C anneal was measured to be $\sim 8.2 \times 10^{-5} \Omega\text{-cm}^2$ for 6H–SiC samples with doping level of $\sim 2 \times 10^{18}$ cm^{-3}.

B. I–V Characteristics

The forward and reverse current–voltage ($I-V$) characteristics measured at different temperatures allow for quantitative determination of Schottky diode parameters such as the Schottky barrier height (ϕ_B), the ideality factor (η), the effective area-Richardson's constant (A^{**}) product, and the series resistance (R_s) of the diodes. The $I-V$ relationship under thermionic emission theory is given by [21]

$$J = J_s[\exp(qV/\eta kT) - 1] \tag{2}$$

and

$$J_s = A^{**}T^2 \exp[-q\phi_B/kT] \tag{3}$$

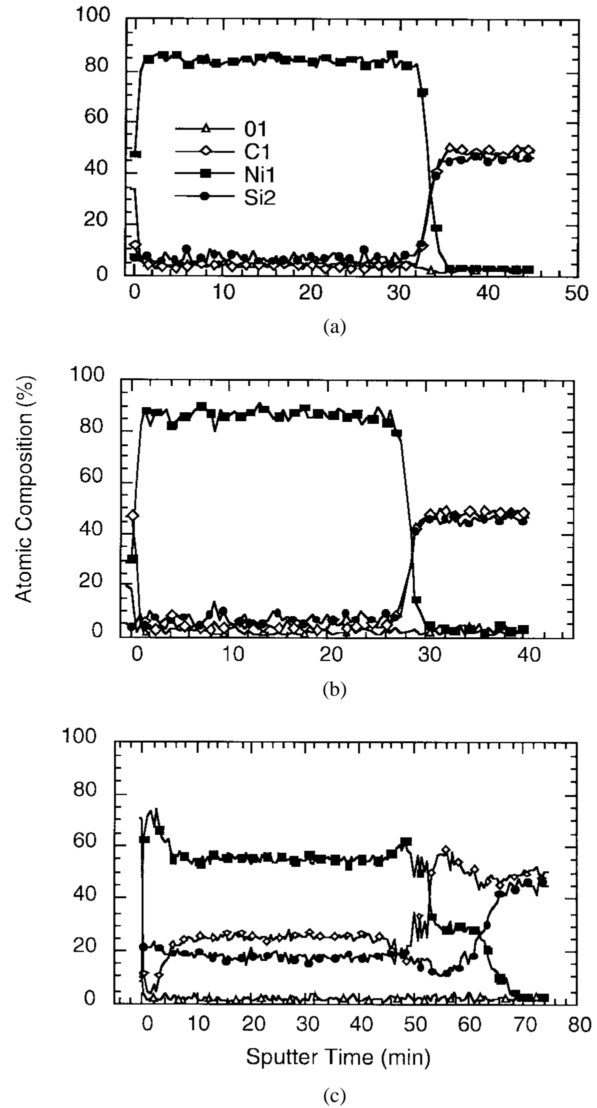


Fig. 3. Auger depth profiles of Ni/6H–SiC structure: (a) as-deposited; (b) annealed at 600 °C, 5 min in Ar; and (c) annealed at 900 °C, 5 min in Ar.

where η is the ideality factor incorporating the tunneling currents in a practical diode. If the applied voltage V is much larger than kT/q, then the exponential term in the above equation dominates, and J can be approximated as

$$J = J_s \exp(qV/\eta kT). \tag{4}$$

η and J_s can thus be determined from the experimentally obtained forward density–voltage ($J-V$) characteristics at a given temperature. J_s can be measured by extrapolating the linear region of the $\ln J$ versus V plot to $V = 0$, and η can be determined by modifying (4) as

$$\eta \equiv q/kT[\delta V/\delta(\ln J)]. \tag{5}$$

The $I-V$ characteristics of Ni/4H–SiC and Pt/4H–SiC Schottky diodes at room temperature are shown in Fig. 5. The doping concentration of the drift region was 6.1×10^{15} cm^{-3}. For the Ni SBD [see Fig. 5(a)], a forward current density (J_F) of 100 A/cm^2 was achieved at a forward voltage drop of 1.78 V. The ideality factor obtained from the slope of the

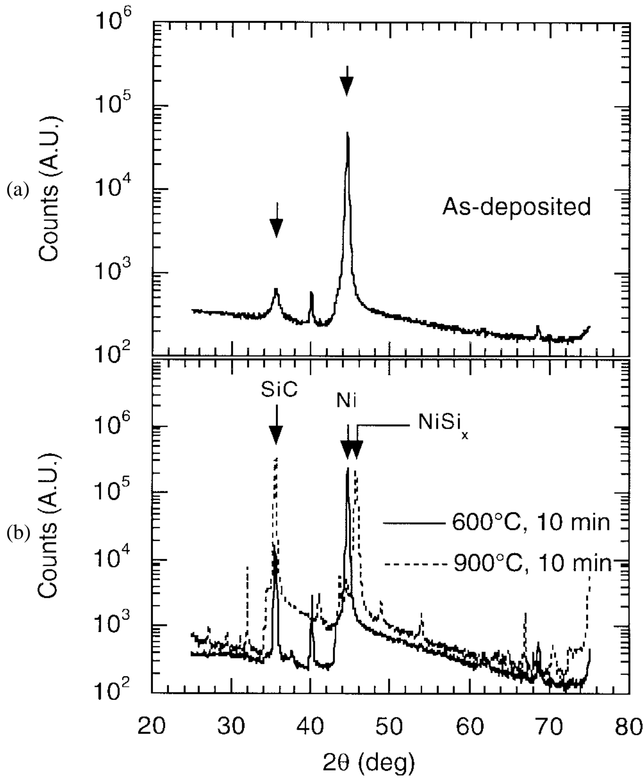


Fig. 4. X-ray diffraction spectra of Ni/6H–SiC sample: (a) as-deposited and (b) after 600 °C and 900 °C anneals.

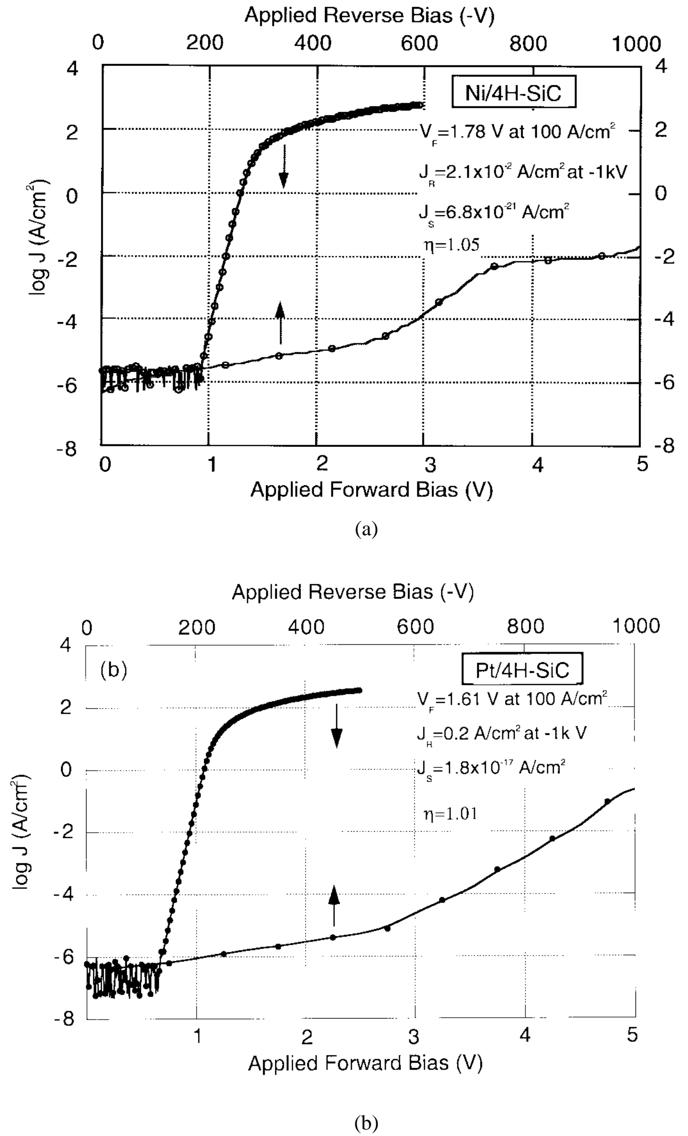


Fig. 5. $I-V$ characteristics at room temperature of 1 kV Schottky diodes; (a) Ni/4H–SiC and (b) Pt/4H–SiC.

forward $J-V$ plot for the Ni/SiC diode was 1.05, and the saturation current density at room temperature, extrapolated from the $\log J$ vs. V plot was determined to be 6.8×10^{-21} A/cm^2. The Schottky barrier height calculated using the theoretically predicted value of the Richardson constant (146 A-cm^{-2}-K^{-2}) [18], was found to be 1.59 eV. The Pt SBD shown in Fig. 5(b) operated at 100 A/cm^2 at a forward voltage drop of 1.61 V, had an ideality factor of 1.01, a saturation current density at room temperature of 1.8×10^{-17} A/cm^2, and a Schottky barrier height of 1.39 eV.

According to Itoh *et al.* [5], the breakdown electric field corresponding to the doping of our drift layer is ~2.7 MV/cm. The punch-through breakdown voltage ($V_{\rm pt}$) for our device is then calculated to be ~2130 V. The Ni/4H–SiC diodes typically had breakdown voltages of 1000 V (~47% of $V_{\rm pt}$), with some diodes as high as 1200 V (~56% of $V_{\rm pt}$). The premature breakdown is possibly due to electric field crowding around the periphery of the devices. This is evident in the following discussion where the leakage current density of the Schottky diodes are found to be dependent on the area/perimeter ratio of the devices. Under reverse bias blocking conditions, a leakage current density of 1.5×10^{-4} A/cm^2 was observed for these diodes at -600 V. The room temperature current ON/OFF ratio corresponding to J_F and J_R at 2 V and -500 V, respectively, was found to be 7.1×10^6. The Pt/4H–SiC diodes had a corresponding ON/OFF ratio of 4.3×10^7.

C. High-Temperature Performance

High-temperature operation of the Schottky diodes on SiC has been investigated. The diodes were tested in a vacuum environment (10 mTorr). The $\log J$ vs. V plots contained in Fig. 6 show a linear regime for a range of applied forward bias voltages at all temperatures for both Ni/ and Pt/4H–SiC diodes. Fig. 7 shows the forward voltage drop for these diodes as a function of temperature corresponding to current densities of 1, 10, and 100 A/cm^2. The reverse bias characteristics of the Ni/4H–SiC diodes as a function of temperature are shown in Fig. 8. A peculiar observation is that the leakage current at 100 °C is lower than at room temperature. This "annealing effect" has been consistently observed in SiC Schottky diodes and could be due to a possible improvement of the metal-SiC interface upon raising the temperature. One possible explanation is that the effective annealing reduces the barrier inhomogenities within the contact area. Increasing the temperature to 200 °C or more leads to an increase in the diode leakage current as predicted by the thermionic emission theory. It is also seen that the current ON/OFF ratio as defined for the 4H–SiC diodes previously does not show a significant reduction with increasing temperatures, and stays in excess of 10^6 for temperatures up to 300 °C.

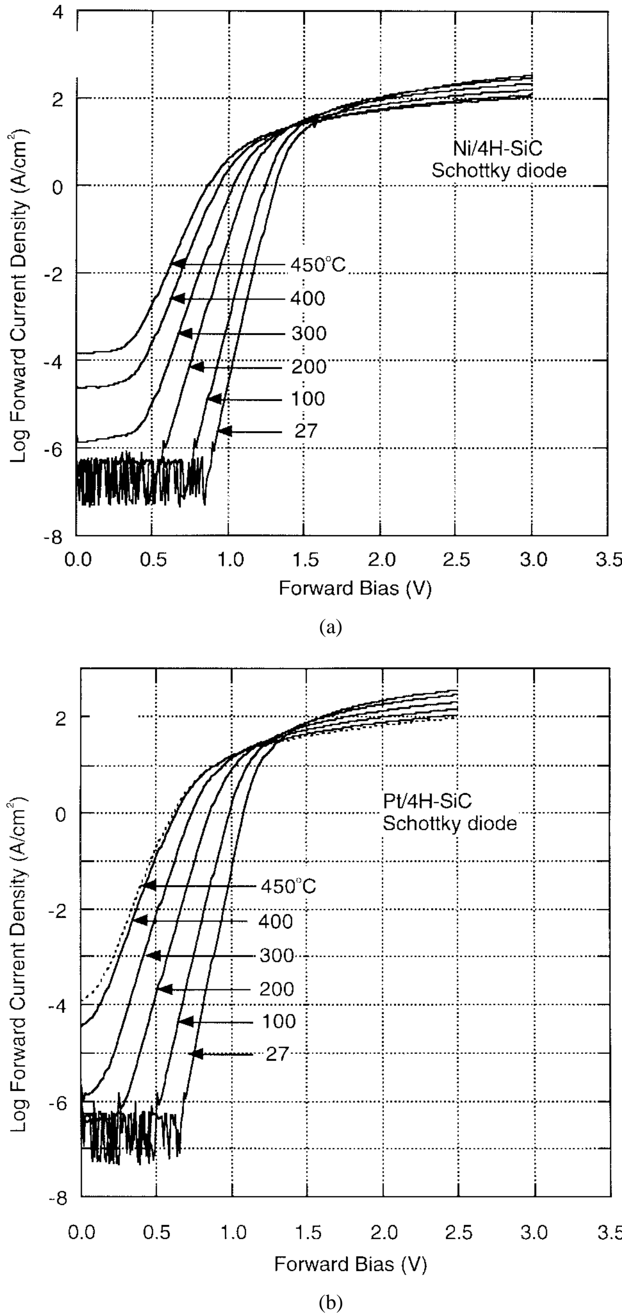


Fig. 6. Forward $I-V$ characteristics as a function of temperature: (a) Ni/4H–SiC Schottky diodes and (b) Pt/4H–SiC Schottky diodes.

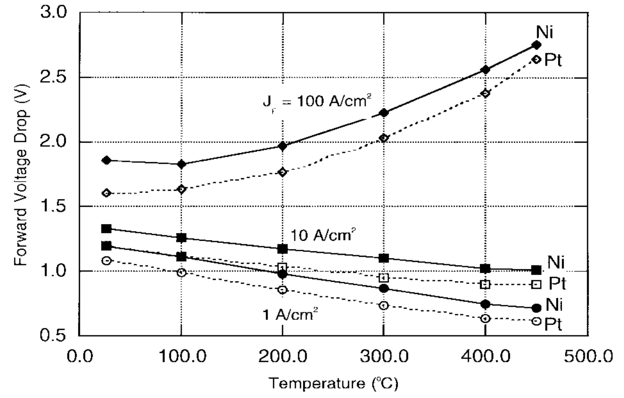


Fig. 7. Forward voltage drop as a function of temperature for different current density levels in a Ni/4H–SiC Schottky diode.

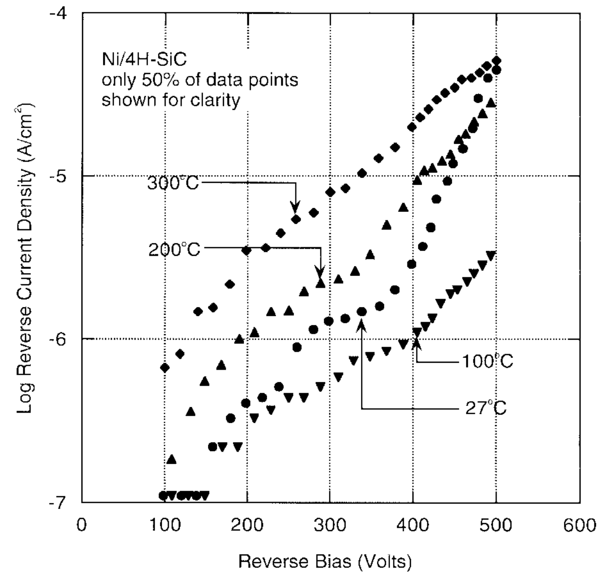


Fig. 8. Reverse $I-V$ characteristics of Ni/4H–SiC Schottky diodes as a function of temperature. For clarity only 50% of the points are shown.

High-temperature forward $J-V$ data was utilized to obtain the Richardson constant and the average Schottky barrier height. These quantities can be found from the y-intercept and the slope of the $\ln(J_s/T^2)$ vs. $1000/T$ plot obtained from the following equation:

$$\ln\left(\frac{J_s}{T^2}\right) = -\frac{q\phi_{Bn}}{k}\left(\frac{1}{T}\right) + \ln(A^{**}). \tag{6}$$

The Richardson plots obtained for both Ni and Pt diodes are shown in Fig. 9. The value of the active-area Richardson constant for Ni and Pt diodes was found from the y-intercept of the $\ln J_s/T^2$ vs. $1/T$ plot to be 1.39×10^{-3} and 3.83×10^{-3} A-cm^{-2}-K^{-2}, respectively. The average value of Schottky barrier height for Ni and Pt was found from the slope of the plot to be 1.37 and 1.15 eV, which is in agreement with the value obtained from the Cheung's $I-V$ method [21] as discussed later. It is important to note that the extracted value of the active area effective Richardson constant has been found to be several orders of magnitude lower than the theoretically predicted value (146 A-cm^{-2}-K^{-2}). The barrier heights for high-voltage SiC Schottky diodes reported in the literature thus far have been calculated using this theoretical value of A^{**} in the $I-V$ analysis. In our calculations, we have utilized the experimental value of the Richardson constant, which is five orders of magnitude lower than the theoretical value. For this reason, our value of the Ni/4H–SiC barrier height is somewhat lower than that reported in the literature. The smaller, experimentally determined value of the Richardson constant indicates that either the effective active area is in fact much smaller than the device area, or that the effects of quantum-mechanical reflection of electrons from the barrier and tunneling of electrons through the barrier must be included in the calculation for A^{**} [22].

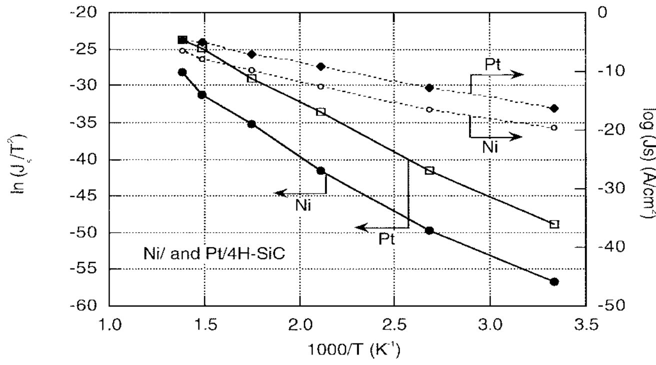


Fig. 9. Richardson plot for Ni/4H–SiC Schottky diodes.

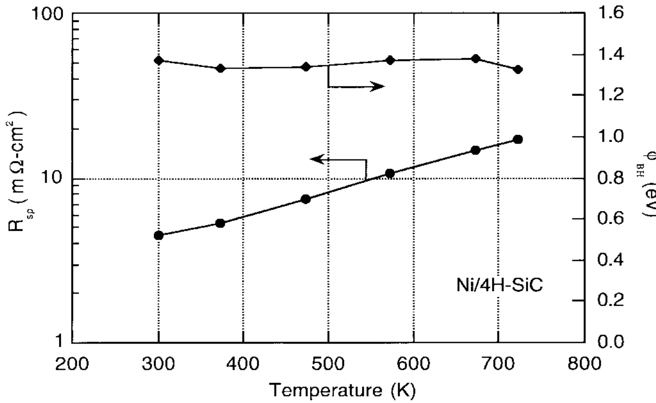


Fig. 10. Series resistance and Schottky barrier height of Ni/4H–SiC diodes as a function of temperature.

The series resistance of the diodes was calculated by applying the method of Cheung and Cheung [21]. The effect of diode series resistance R is usually modeled by a series combination of an ideal diode and a resistance R through which the current flows. For an applied forward bias, $V_D > 3kT/q$, the forward $J-V$ characteristics of a Schottky diode obeying the thermionic emission model can be written as [21]

$$J = J_s \exp[q(V - JR_{\rm sp})/\eta kT] \tag{7}$$

where J_s was defined in (3) and $R_{\rm sp}$ is the specific on-resistance of the diode. Upon differentiating V with respect to J in (7) and rearranging the terms, the following relationship can be obtained:

$$\frac{d(V)}{d(\ln J)} = R_{\rm sp}J + \frac{\eta kT}{q}. \tag{8}$$

Plotting $d(V)/d(\ln J)$ versus J, the slope of the straight line gives the specific series resistance, $R_{\rm sp}$, and the y-axis intercept gives the ideality factor η. The Schottky barrier height is evaluated by defining a function $H(J)$ given by [21]

$$H(J) \equiv V - (\eta kT/q)\ln(J/A^{**}T^2). \tag{9}$$

Applying (7), $H(J)$ can be deduced as

$$H(J) = R_{\rm sp}J + \eta\phi_b. \tag{10}$$

The plot of $H(J)$ versus J thus gives a straight line which intercepts the y axis at $\eta\phi_b$. Using the ideality factor value extracted from the $d(V)/d(\ln J)$ vs. J plot, the barrier height can be determined. The slope of the plot of $H(J)$ vs. J also provides an alternative determination of $R_{\rm sp}$, which was found to be very close to that obtained from (9), thus establishing the consistency of this approach.

Fig. 10 shows the dependence of the specific on-resistance and Schottky barrier height for the Ni/4H–SiC diodes as a function of temperature. $R_{\rm sp}$ at room temperature was found to be 4.49 mΩ-cm^2, increasing to 17.09 mΩ-cm^2 at 450 °C. A curve fit of the $R_{\rm sp}$ data indicates a $T^{1.6}$ temperature dependence, similar to that observed by Itoh *et al.* [24] for Ti/4H SiC Schottky diodes. The barrier height does not show a significant variation with temperature, with values of 1.38 and 1.33 eV at 25 °C and 450 °C, respectively. This is expected from theory since the bandgap of SiC changes very slightly within the temperature range investigated.

1) Current Density Dependence on Diode Area To investigate the effect of diode area on the current density, we have tested circular diodes with diameters varying from 30 to 200 μm. The effect of area/perimeter ratio on diode current density is shown in Fig. 11. For a more accurate determination of this effect, we have included the results from 16 diodes on two different dies on the chip. As seen in Fig. 11(a), increasing the area/perimeter ratio reduces the current density during forward bias. In Fig. 11(b), the plot of normalized reverse current density as a function of the area/perimeter ratio shows a decreasing trend with increasing diameter of the devices. This indicates the larger diameter devices are necessary to remove the perimeter effects. It is important to mention though that the high defect density in the currently available SiC wafers considerably reduces the yield if we have very large area devices on the chip.

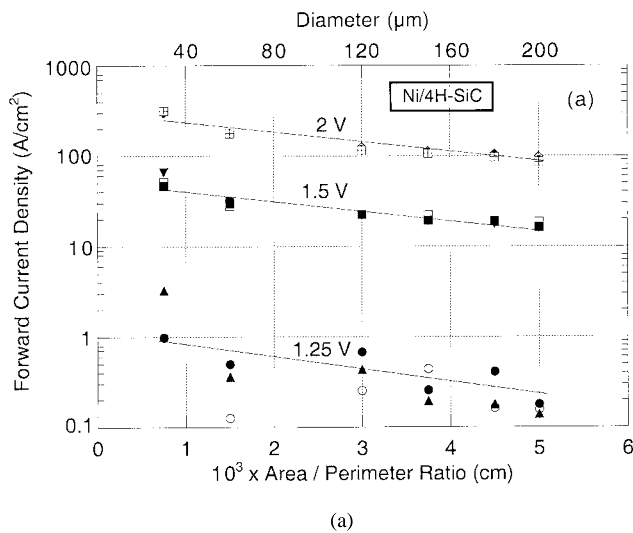
D. C–V Characteristics

The Schottky barrier height of the Ni/4H–SiC Schottky diodes has also been determined using the capacitance–voltage ($C-V$) technique. Fig. 12 shows the plot of the square of the inverse of the capacitance per unit area (A/C)^2 as a function of applied voltage for a Ni/4H–SiC SBD at room temperature. The voltage intercept gives a built-in potential of 1.32 V at 27 °C. The built-in potential is related to the barrier height by the relationship

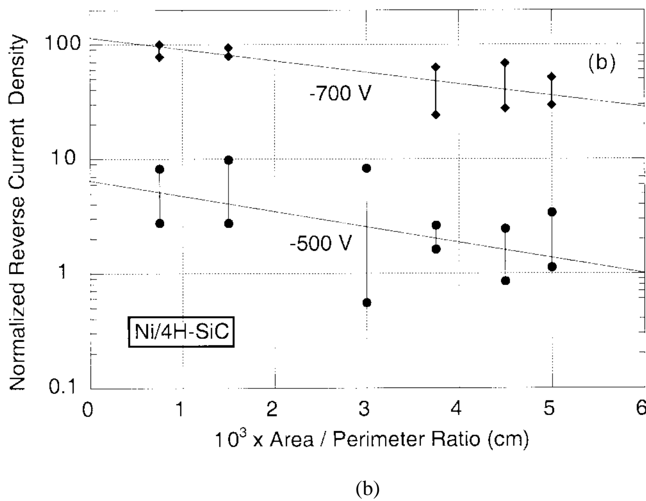
$$\phi_b = -V_i + V_0 + kT/q \tag{11}$$

$$V_0 = (kT/q)\ln(N_C/N_D) \tag{12}$$

where N_C is the effective density of states in the conduction band, and N_D is the donor concentration. For SiC material with donor concentration of 5×10^{15} cm^{-3}, V_0 is estimated to



(a)



(b)

Fig. 11. Dependence of current density on diode area/perimeter ratio: (a) forward bias and (b) reverse bias.

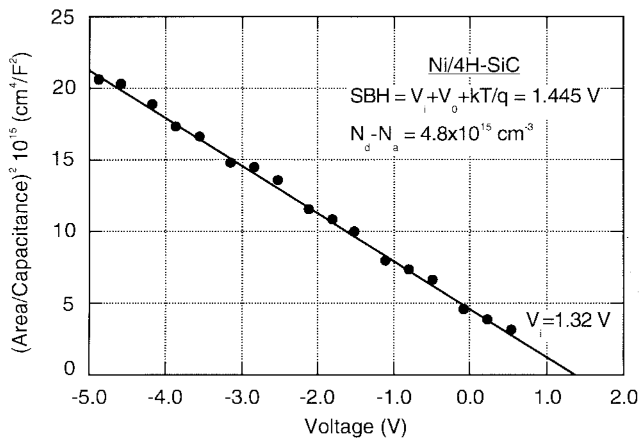


Fig. 12. Capacitance–voltage characteristics of a 200-μm Ni/4H–SiC Schottky diode.

be approximately 0.1 V. The room temperature barrier height calculated using (12) is 1.445 eV.

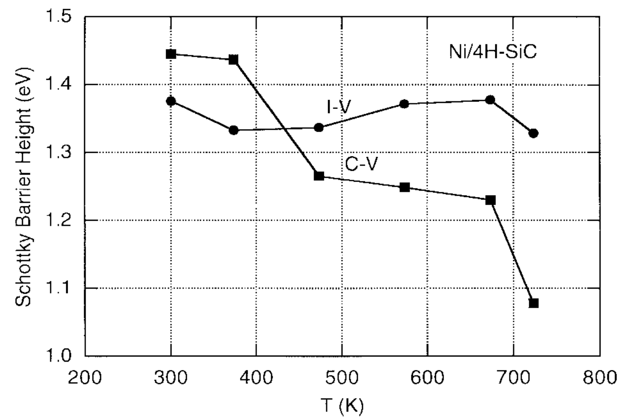


Fig. 13. Schottky barrier height of a 200-μm Ni/4H–SiC Schottky diode determined from the $I-V$ and $C-V$ methods as a function of temperature.

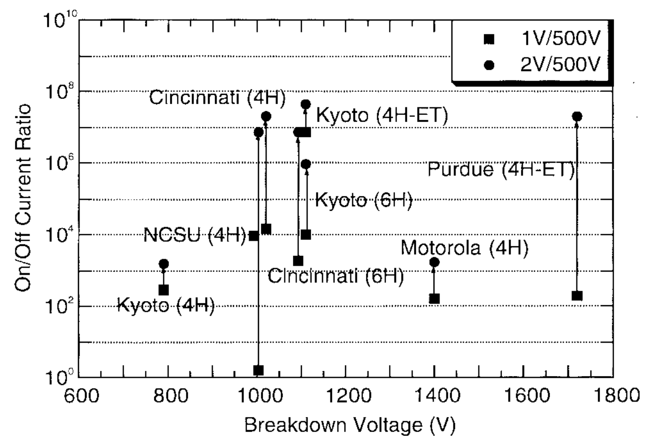


Fig. 14. Summary of published ON/OFF ratios versus breakdown voltages for high-voltage SiC Schottky rectifiers.

The $C-V$ characteristics of the diodes were also measured as a function of temperature and the built-in potential was extracted from the plots for each temperature. The Schottky barrier height (SBH) was thus determined as a function of temperature using (11). The SBH measured from the $C-V$ data (Fig. 13) decreases with temperature from 1.45 at room temperature to 1.26 eV at 200 °C, and 1.08 eV at 450 °C. The $C-V$ plots at different temperatures were parallel to one another to a good approximation, thus indicating that the net carrier concentration remains unaffected up to 450 °C.

V. Summary and Conclusions

SiC Schottky barrier diodes have been shown to exceed the performance of Si-based counterparts for applications requiring high-power and high-temperature operation, and could rapidly become commercially viable as an attractive alternative to the slower Si-based p–i–n diodes currently being used in several power electronics applications. Over the past six years or so, several other groups have investigated high-voltage (>100 V) Schottky diodes on SiC [6]–[8], [16]–[18], and [24]–[29]. The various device approaches and resulting characteristics are summarized in Table V of the review by Saxena and Steckl [23].

A useful figure of merit for rectifiers is the ON/OFF current ratio, which combines the current-carrying capability in forward bias with the leakage current in reverse bias. The Ni– and Pt–SiC Schottky barrier diodes which we have fabricated utilizing the metal field plate termination have yielded ON/OFF current ratios between 10^6 and 10^7 at room temperature. These diodes have been tested at elevated temperatures and show satisfactory operation at least up to 300 °C, where they exhibit an ON/OFF ratio that is still in excess of 10^6. A summary of published ON/OFF ratios for 4H and 6H SiC SBD's utilizing various metals and structures is shown in Fig. 14 as a function of reported breakdown voltage. This summary was only able to include results where all the necessary characteristics (forward current, leakage current and breakdown voltage) were available in the published literature. As can be seen ON/OFF ratios of one million or more have been obtained by several groups for diodes with breakdown voltages of ~1000 to 1100 V. SiC SBD's are also likely to allow operation beyond 300 °C, which is the upper limit of Si SOI-based devices.

ACKNOWLEDGMENT

The authors would like to acknowledge many useful discussions with P. G. Neudeck and J. Scofield.

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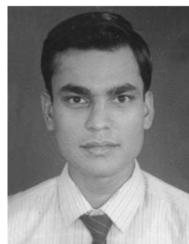

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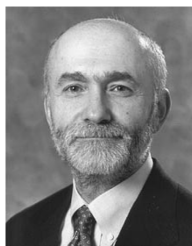

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