SiC/Si Heterojunction Diodes Fabricated by Self-Selective and by Blanket Rapid Thermal Chemical Vapor Deposition

P. H. Yih, J. P. Li, and A. J. Steckl

Abstract—**SiC/Si heterojunction diodes have been fabricated by two different rapid thermal chemical vapor deposition (RTCVD) processes: a localized self-selective growth and blanket growth. The self-selective growth of crystalline cubic (β) SiC was obtained by propane carbonization of the Si substrate in regions unprotected by an SiO_2 layer, producing planar diodes. Mesa diodes were fabricated using the blanket growth of polycrystalline β-SiC produced by the decomposition of methylsilane (CH_3SiH_3). The SiC/Si heterojunction diodes show good rectifying properties for both device structures. Reverse breakdown voltage of 50 V was obtained with the self-selective SiC/Si diode. The mesa diodes exhibited even higher breakdown voltages (V_{br}) of 150 V and excellent ideality factors of 1.06 at 25°C. The high V_{br} and good forward rectifying characteristics indicate that the SiC/Si heterojunction diode represents a promising approach for the fabrication of wide-gap emitter SiC/Si heterojunction bipolar transistors.**

I. Introduction

THE combination of SiC films with Si technology holds the promise for opening up new electronic applications in areas requiring high power, high speed, and high temperature. In addition to a wide energy band-gap, SiC has many other useful material properties, including high electric field breakdown, high electron saturation velocity, high thermal conductivity, and high physical and chemical stability [1]. SiC/Si heterojunction diodes (HJD) reported to date [2]–[4] have exhibited low breakdown voltage of only 4 V [2], and a high reverse leakage current density of 5×10^{-4} A/cm^2 at 1 V reverse bias [4], possibly due to the SiC thin film deposition method and/or to the high Si substrate doping. An amorphous $Si_{0.88}C_{0.12}$/Si diode has also been reported to result in a similarly low breakdown voltage and an extremely high reverse leakage current density of 2 A/cm^2 at 1 V reverse bias [5]. Significant improvements in both of these aspects of the SiC/Si HJD are necessary for practical application [6].

In this paper, we present SiC/Si HJD's fabricated by two different SiC growth processes, both of which result in significantly improved electrical characteristics. Due to the large lattice mismatch (20%) between Si and cubic β-SiC, a buffer (or carbonization) layer is necessary for the subsequent growth of a crystalline SiC film [7], [8]. Carbonization layer growth employs the reaction of a hydrocarbon precursor [9], [10] with the Si substrate surface to form a thin SiC film. Carbonization layers consisting of crystalline β-SiC have been successfully grown on Si by rapid thermal chemical vapor deposition (RTCVD) at about 1300°C [11]. RTCVD growth is advantageous in this process in order to minimize the thermal budget. In the first HJD process we have used *self-selective* carbonization growth of SiC by RTCVD, with SiO_2 as the growth masking layer. This is a very simple SiC growth process, using only the pyrolysis of propane (C_3H_8) [11] or other hydrocarbon gas precursors [12], which can be easily integrated with conventional Si technology by the addition of a single step.

The second SiC/Si HJD fabrication process uses low (900°C) temperature, non-selective growth of SiC from organosilane precursors. Organosilanes, such as dimethyldichlorosilane [13], methyltrichlorosilane [14], tetramethylsilane, diethylsilane, tripropylsilane [15], silacyclobutane [16], and methylsilane [17] usually produce polycrystalline SiC films at growth temperatures in excess of 1000°C. We have utilized non-selective methylsilane-grown polycrystalline SiC films to fabricate mesa HJD structures. Growth of unintentionally-doped SiC films on p-Si has been used for both processes. Rectifying I-V characteristics were obtained for both device structures.

II. Experimental Procedures

A. Fabrication of SiC/Si Diodes with the Self-Selective SiC Process

The self-selective SiC/Si heterojunction diodes have been fabricated by growing unintentionally doped SiC on 7–10 Ω-cm ($\sim 10^{15}$ cm^{-3}) p-type Si (100) substrates using an RTCVD system. The RTCVD process for SiC-on-Si growth is described in detail elsewhere [11]. For the self-selective SiC/Si process, the monocrystalline SiC layers were grown at 1300°C for 90 s under both atmospheric and low (5 Torr) pressures by chemically converting the Si substrate surface using C_3H_8 and 0.9 lpm H_2 carrier gas. The propane flow rate was varied from 10 to 100 sccm. In-situ cleaning was performed in the growth

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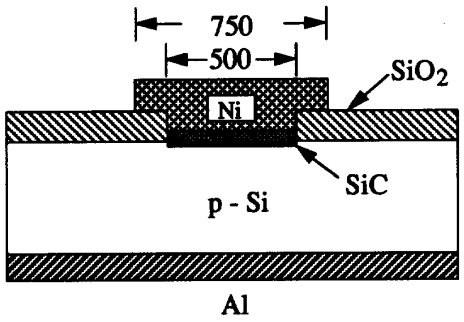


Fig. 1. Schematic diagram of SiC/Si heterojunction diode obtained by selective carbonization (unit: μm).

chamber at 950°C for 3 min in 1.2 lpm H_2 ambient. The SiC film thickness ranges from 100 to 3000 Å depending on C_3H_8 flow rate and growth pressure [18]. The formation and density of voids in the Si substrate depend mainly on the C_3H_8 fraction of the total gas flow [19].

No SiC nucleation was observed on the thermal SiO_2 layer used as the SiC growth mask. By comparison, the conventional selective growth of either Si (homoepitaxy) [20] or SiC (heteroepitaxy) on Si [21, 22] requires the addition of chlorinated gases to the normal precursors to prevent nucleation from occurring on the SiO_2 mask. The schematic diagram of the self-selective n-SiC/p-Si HJD is shown in Fig. 1. The area of the HJD is 500 × 500 μm^2. For ohmic contact to the SiC layer we have utilized a Ni film, annealed in Ar at 900°C for 2 min after deposition. The back-side contact to the Si was Al, annealed at 450°C for 3 min. Both metals were sputter deposited with a thickness of 4000 Å. The process flow for the fabrication of the HJD using the self-selective growth process is shown in Fig. 2.

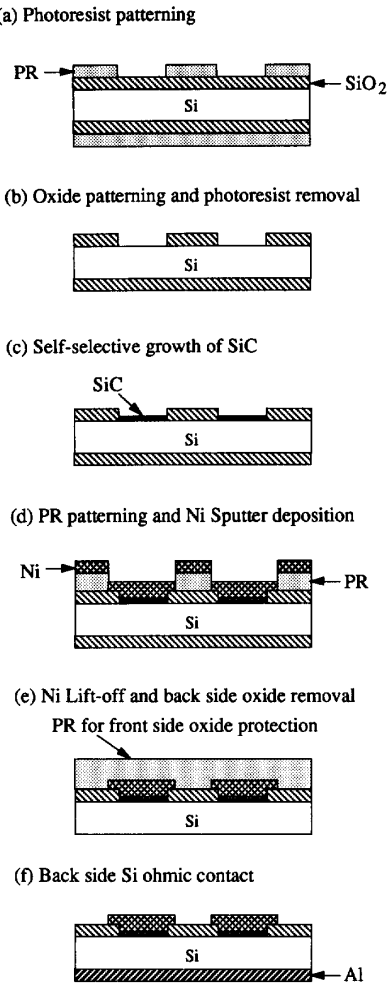


Fig. 2. Process flow for the fabrication of self-selective SiC/Si heterojunction diodes.

B. Fabrication of SiC/Si Diodes with the Blanket SiC Process

The mesa SiC/Si heterojunction diodes have been fabricated by growing unintentionally doped SiC on 7–10 Ω-cm p-type Si (111) substrates using the same RTCVD system. Generally, the base impurity profiles of HBT's can be affected by the high growth temperature of the self-selective process, even though its effect is greatly reduced by the RTCVD approach. For this reason we have also investigated a lower temperature SiC deposition process. This process utilizes organosilane precursors, which contain both Si and C, and results in a blanket deposition of SiC over the whole Si wafer. No carbonization step was included in this process. The schematic diagram of the polycrystalline β-SiC on p-Si HJD fabricated with this non-selective process is shown in Fig. 3. A mesa structure was used to define the junction area. The related process flow for device fabrication using blanket SiC growth is shown in Fig. 4. The SiC films were grown on Si at 900°C and 5 Torr using methylsilane (CH_3SiH_3) and 1.9 lpm H_2 as the carrier gas. After sample loading in the growth chamber and prior to deposition, in-situ cleaning was performed at 900°C in H_2 ambient for 3 min. It has been previously reported that methylsilane, which has a gas phase ratio of Si to C of 1:1, results in Si-rich SiC films at all growth temperatures of 650 to 1050°C [16]. Structural analysis indicates that SiC films grown with our system are polycrystalline. The Auger analysis of the films showed that the Si:C ratio ranges from 1:1 to 1.2:1. No voids were formed in the Si substrate under the methylsilane-grown SiC film. The thickness of the SiC layer deposited by this process is linearly proportional to the concentration of methylsilane in the total gas stream. SiC films of 1.2 μm were used for the fabrication of devices by this process.

Due to the chemical stability of SiC, reactive ion etching (RIE) was used for the patterning of the SiC layer [23] deposited by methylsilane. A sequential combination of two etching gases, NF_3 followed by CHF_3/80% O_2, was used for the SiC etching. The etching conditions for both gases are an RF power of 200 W, a pressure of 20 mTorr, and a total flow rate of 20 sccm. A patterned Al thin film was used as the etching mask. The etch times are determined by the thickness of the methylsilane-grown SiC films. The reasons for using this combination of two etching gases are as follows: (a) pure NF_3

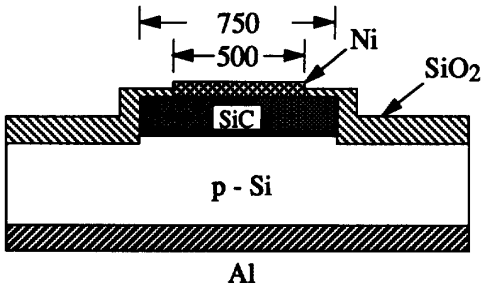


Fig. 3. Schematic diagram of mesa SiC/Si heterojunction diode obtained by methylsilane (unit: μm).

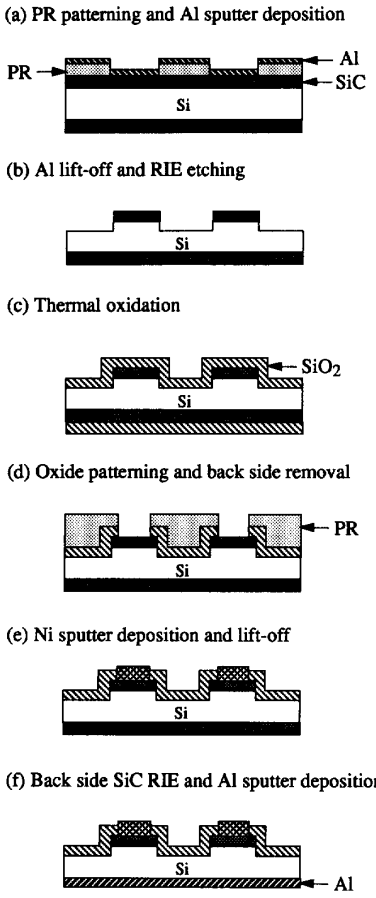
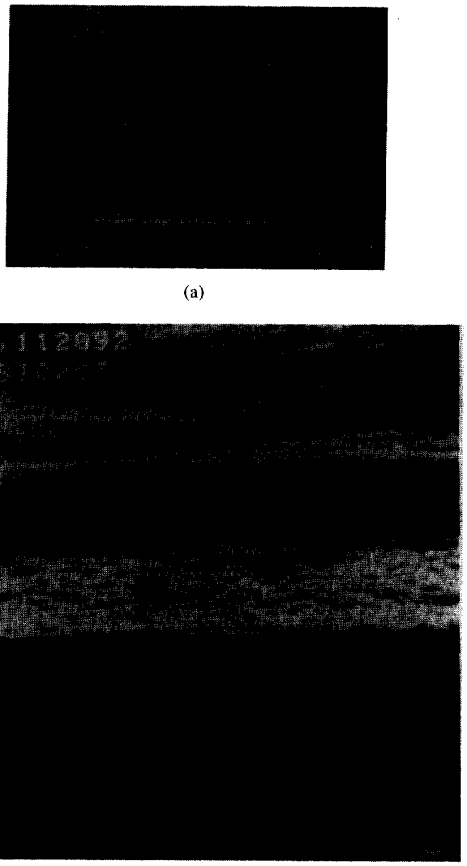


Fig. 4. Process flow for the fabrication of mesa SiC/Si heterojunction diodes.

plasma with its high SiC etch rate allows for an increase in process throughput, while providing a relatively clean etched surface (with occasional spikes); (b) following NF_3 plasma etching, the CHF_3/80% O_2 plasma exhibits an etch selectivity of SiC-to-Si higher than unity [23] and provides the necessary control at the SiC-Si interface. The area of the blanket HJD is 750 × 750 μm^2. As shown in Fig. 4(c), thermal oxide was grown to passivate the device surface after mesa etching. The SiC layer grown on the back-side of the substrate was removed by RIE etching with CHF_3/50% O_2 plus 4 sccm H_2



(a)

(b)

Fig. 5. Microphotographs of a self-selective SiC/Si heterodiode: (a) top view; (b) cross-section.

under the following conditions: 200 W RF power, 25 mTorr pressure, and 24 sccm total flow rate. This provides a residue-free [24], [25] etched surface to be used for the Si ohmic contact. Ohmic contacts to SiC and Si are fabricated in the same way as described above for the self-selective process.

III. Results and Discussion

A. Self-Selective SiC/Si Diode

The top view and cross-section microphotographs of a SiC/Si HJD fabricated with the self-selective SiC growth process are shown in Fig. 5(a) and 5(b), respectively. For the cross-sectional view, the samples were dipped in a KOH/IPA solution at 80°C for 30 s in order to be able to distinguish the SiC-Si interface [26]. As seen in Fig. 5(b), the etchback of the Ni film and of the Si substrate clearly reveals the unaffected and, hence, exposed SiC layer.

The current density-voltage (J-V) characteristic of the self-selective SiC/Si HJD is plotted in Fig. 6. A diode rectification ratio of forward to reverse current (always defined at ± 1 V bias) of 1.6 × 10^4 is obtained at room temperature. The diode exhibits a relatively high reverse breakdown voltage

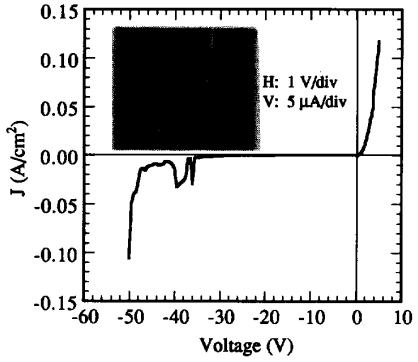


Fig. 6. J-V characteristics of self-selective SiC/Si heterodiode. Insert indicates the forward I-V characteristic.

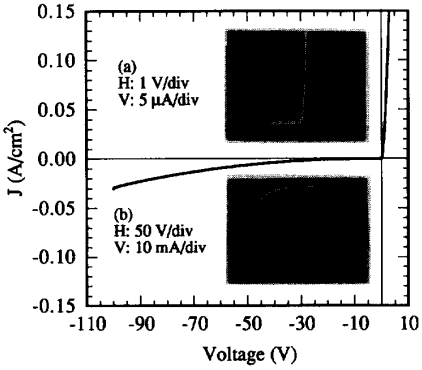


Fig. 8. J-V characteristics of blanket SiC/Si heterodiode. Inserts indicate (a) the forward I-V characteristics; (b) the reverse breakdown voltage of 150 V.

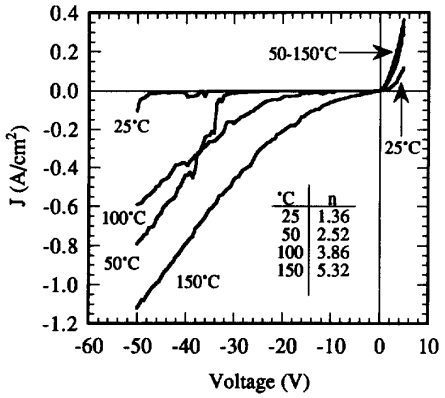


Fig. 7. J-V characteristics of self-selective SiC/Si heterodiode at different temperatures.

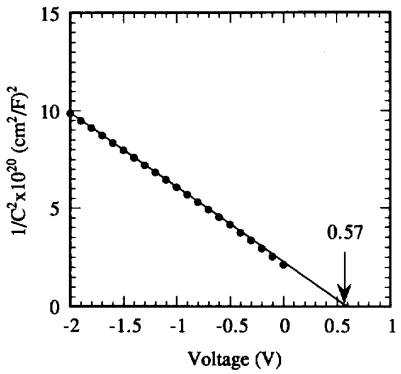


Fig. 9. C-V characteristics of blanket SiC/Si heterodiode.

of approximately 50 V. Leakage current densities of 10 and 15 μA/cm^2 have been measured at 1 and 10 volts reverse bias, respectively. The inset photograph in Fig. 6 shows the I-V characteristic of the self-selective SiC/Si HJD at low voltage and current of 1 V/div and 5 μA/div, respectively. The forward bias ideality factor of HJD is 1.36, indicating significant diffusion and recombination currents [27].

The J-V characteristics of the HJD taken at different temperatures are shown in Fig. 7. As expected, the increase in temperature caused an increase in leakage current and a decrease in the effective breakdown voltage. The temperature effect of the self-selective HJD indicates that the junction breakdown has a negative temperature coefficient, which is dominated by the tunneling mechanism [27]. This is in contrast to avalanche breakdown which exhibits a positive temperature coefficient, with the breakdown voltage increasing with temperature. At 150°C, the rectification ratio decreases to 2.4.

B. Blanket SiC/Si Diode

The room temperature J-V characteristic of the blanket SiC/Si diode is shown in Fig. 8. A relatively high current rectification ratio of 2×10^4 is obtained for the mesa SiC/Si diode at 25°C. Leakage current densities have been measured at 1 and 10 volts reverse bias to be 15 μA/cm^2 and 0.3 mA/cm^2, respectively. In the forward bias region, the maximum current measured (10 mA) is limited by the H-P 4140 current meter. The reverse current gradually increases with increasing reverse bias. The insert photographs in Fig. 8 are: (a) the diode I-V characteristic with horizontal and vertical scales of 1 V/div and 5 μA/div, respectively; the forward bias ideality factor of the blanket SiC/Si HJD is 1.05, which indicates that the diffusion current mechanism dominates [27]; (b) the reverse bias characteristics only with horizontal and vertical scales of 50 V/div and 10 mA/div, respectively; hard breakdown is observed at about 150 V reverse bias.

The $1/C^2$ versus V data of Fig. 9 reveal a linear relationship indicating that the abrupt junction model is applicable to the blanket SiC/Si HJD structure. A built-in voltage (V_{bi}) of 0.57 V is obtained. The effect of temperature on the J-V characteristics of the blanket HJD is shown in Fig. 10. Over the temperature range of 25 to 100°C, the ideality factor is observed to increase with temperature from 1.06 to 2.88. At 100°C, the current rectification ratio decreases to a value of 500. Slightly rectifying characteristics were measured at an ambient temperature of 220°C, with a rectification ratio of 2.7.

C. Device Modeling

The charge carrier current mechanisms in the SiC/Si heterojunction diode are considerably more complex than those of a

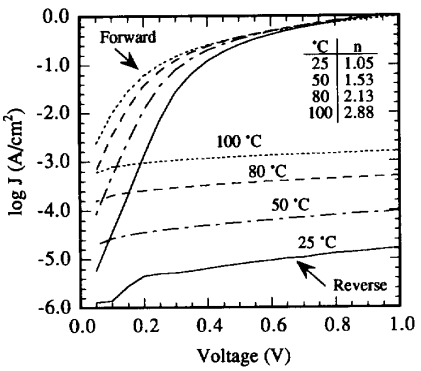


Fig. 10. J-V characteristics of blanket SiC/Si heterodiode at different temperatures.

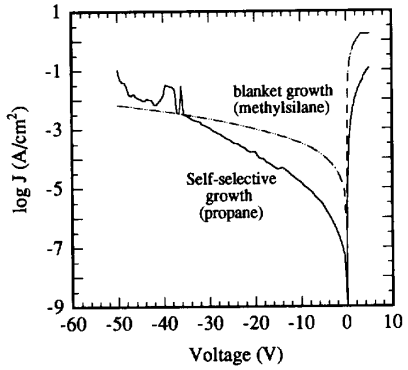


Fig. 11. Comparison of J-V characteristics for self-selective and blanket SiC/Si heterojunction diodes at room temperature.

Si p-n junction. A multi-tunneling capture-emission (MTCE) model has been proposed [28] to explain the voltage and temperature dependence of the current in the n-amorphous/p-crystalline Si heterojunction, where a large valence band discontinuity results in a large barrier to hole flow. In the MTCE model, under forward bias a hole in the valence band of the crystalline p-Si hops from one localized state to another in the amorphous Si. This multi-tunneling process continues until the rate of hole release into the valence band or of recombination with an electron in the conduction band becomes greater than the tunneling rate. This mechanism has been shown to apply [29] to the n-SiC/p-Si HJD, where the energy band diagram is quite similar to that of n-amorphous/p-crystalline Si heterojunction.

Using the MTCE model, the diode current-voltage relation can be described by the following expressions: (a) forward bias: $I_F = I_o e^{AV} = e^{(-\Delta E_{\rm af}/k_B T)} \times e^{AV}$; (b) reverse bias: $I_R = e^{(-\Delta E_{\rm ar}/k_B T)} \times (V_{\rm bi} - V)^{1/2}$. $\Delta E_{\rm af}$, A, and $\Delta E_{\rm ar}$ are constants independent of temperature and voltage. k_B and T are Boltzmann's constant and the temperature, respectively. Based on the values of the ideality factor, the forward bias current of the self-selective and blanket growth HJD is a combination of diffusion and recombination currents. For the blanket growth HJD, the forward bias current is dominated by diffusion current. Theoretically, since SiC and Si have small values of n_i (SiC = 3.11 cm^{-3} and Si = 1.45 $\times$ 10^{10} cm^{-3}), the generation current may dominate the reverse current at room temperature [27]. A comparison of J-V characteristics of self-selective and blanket HJD's at room temperature is shown in Fig. 11. The reverse bias current density (J_R) shown in Fig. 11 for both devices structures exceeds the values of reverse saturation current density (J_o). This indicates that the reverse current is limited by other transport mechanisms, which can be described as $J_R \sim e^{(-\Delta E_{\rm ar}/k_B T)}$. The reverse saturation current is determined by extrapolating the forward bias current to zero bias. The activation energies for the self-selective growth SiC/Si diode are obtained from the Arrhenius plot in Fig. 12(a): 1.1 eV for of $\Delta E_{\rm af}$ and 0.9 eV for $\Delta E_{\rm ar}$ at reverse bias of -5 V. Considerably lower activation energies are obtained for the blanket growth SiC/Si HJD (see Fig. 12(b)): 0.70 eV for $\Delta E_{\rm af}$ and 0.39 eV for $\Delta E_{\rm ar}$ at reverse bias of -5 V.

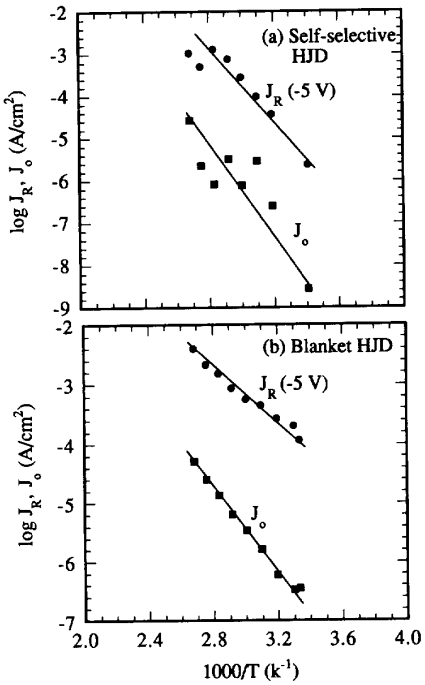


Fig. 12. Arrhenius plot of saturation current (I_o) and reverse-bias current (I_R) at -5 V for (a) self-selective SiC/Si HJD; (b) blanket growth SiC/Si HJD.

IV. Conclusion

SiC/Si heterojunction diodes have been successfully fabricated using self-selective and blanket deposition processes. Self-selective planar diodes were grown by propane with SiO_2 as the growth mask. No SiC nucleation was observed on the thermal SiO_2 mask layer. Blanket growth mesa diodes were grown by an organosilane precursor (CH_3SiH_3). The room temperature ideality factors of planar and mesa HJD's are 1.36 and 1.05, respectively. The mesa diodes also exhibit a high rectification ratio of 2 $\times$ 10^4 at $\pm$ 1 volts bias at 25°C. A high breakdown voltage of 50 V was obtained with the planar diodes. Even higher values of $V_{\rm br}$ were obtained with

the mesa diodes, 150 V at 25°C. The temperature effect on the J-V characteristics of the device structure was studied. Rectifying characteristics for the planar and mesa HJD's are observed up to ambient temperatures of 150 and 220°C, respectively. In conclusion, significant improvement in the SiC/Si heterojunction diodes have been established, enabling the fabrication of SiC/Si diodes and heterojunction bipolar transistors.

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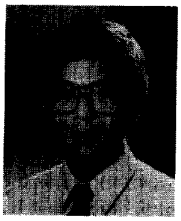

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