Electrical Properties of Si p⁺–n Junctions for Sub-0.25 μm CMOS Fabricated by Ga FIB Implantation

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Abstract—p⁺–n junction diodes for sub-0.25 μm CMOS circuits were fabricated using FIB Ga implantation into n-Si (100) substrates with background doping of Nₓ = (5–10) × 10¹⁵ cm⁻³ and Nₛ = (1–10) × 10¹⁷ cm⁻³. Implant energy was varied from 2 to 50 keV at doses ranging from 1 × 10¹⁴ to 1 × 10¹⁵ cm⁻² with different scan speeds. RTA was performed at either 600°C or 700°C for 30 s. Diodes fabricated on Nₛ with 10 keV Ga⁺ exhibited a leakage current (Iₜₐₜ) 100× smaller than those fabricated with 50 keV Ga⁺. Tunneling was determined to be the major current transport mechanism for the diodes fabricated on Nₛ substrates. An optimal condition for Iₜₜ on Nₛ substrates was obtained at 15 keV/1 × 10¹⁵ cm⁻². Diodes annealed at 600°C were found to have an Iₜₜ 1000× smaller than those annealed at 700°C. I–V characteristics of diodes fabricated on Nₛ substrates with low energy Ga⁺ showed no implant energy dependence. I–V's were also measured as a function of temperature from 25 to 200°C. For diodes implanted with 15 keV Ga⁺, the cross-over temperatures between Iₜₜ and Iₜₜ occurred at 100°C for Nₛ and at 91°C for Nₛ substrates. A combination of low energy/high dose implantation was found to be advantageous since low energy ions create less damage, which in turn is easier to anneal out.

I. INTRODUCTION

DEMANDS of shrinking device geometries require that new techniques be designed in order to form ultrashallow p⁺–n junctions. Shankage in the lateral dimensions of the MOSFET design must be accompanied by a corresponding reduction in the vertical dimension, otherwise short channel effects will degrade the subthreshold characteristics as well as the stability of the threshold voltage to gate-length variation. A major issue with shrinking the channel length of a MOSFET is the overlap of the space charge regions associated with the source-substrate and drain-substrate junctions. Since the depletion regions (drain and source) extend deep into the lightly doped substrate, there is a possibility of bulk punchthrough of the drain to the source when these space-charge regions overlap. To prevent punchthrough effects in short-channel devices, one has to increase the substrate doping. As the gate length approaches the 0.1 μm regime, the required junction depth is estimated to be approxi-
mately 30 nm and the required channel doping approaching 10¹⁸ cm⁻³ [1]. A disadvantage of this high channel doping lies in the fact that the drain current is now dominated by the tunneling mechanism [2], [3].

Focused ion beam (FIB) implantation is a developing technology [4] that has the advantage of localized processing which can tailor the implant conditions for a particular device. FIB implantation, being a direct-write, maskless, and resistless technique, is ideally suited for fast turnaround (albeit low volume) processing. FIB systems are also more flexible than conventional ion implanters with respect to acceleration energy, especially in terms of operating at low energies. Selection of Ga as a p-dopant provides the advantage of fabricating nanoscale junctions at low energies [5] with minor channeling [6], as well as maintaining a low thermal budget. In this paper, we report on the electrical characteristics of p⁺–n shallow junctions fabricated with Ga FIB implantation into substrates with low background resistivity, thereby effectively simulating high channel doping conditions compatible with sub-0.25 μm CMOS technology.

II. EXPERIMENTAL

n-Si wafers with (100) orientation and background doping (phosphorus) concentration of (5–10) × 10¹⁵ cm⁻³ and (1–10) × 10¹⁷ cm⁻³ were employed for device fabrication. A thermal oxide of 200 nm was grown to isolate the diodes. A two-mask process was used in conjunction with Al liftoff for the contacts. After liftoff, the Al was sintered at 300°C for 9 min to improve the electrical contact, while still avoiding Al spiking of the junction.

The Ga⁺ ion implantation was performed perpendicular to the substrates using a focused ion beam system. The operation of the FIB system for the purpose of shallow junction fabrication was previously described in [5]. The current density available in FIB implantation depends upon the implantation current and the beam size. Implantations for these experiments were performed with a Ga⁺ current of 300 pA. The beam diameter ranged from 1000 nm for a 5 keV beam to 200 nm for the 50 keV beam, thereby giving a current density ranging between 40 and 1000 mA/cm². An implantation area of 540 × 540 μm² was selected for these experiments as a compromise between implant time and area required for various measurements.
The experiments were carried out with a Ga liquid metal ion source containing the natural distribution of isotopes and, hence, ionized species [5]. Single serpentine scan was used to provide doses ranging from $1 \times 10^{13}$ to $1 \times 10^{15}$ cm$^{-2}$. Implants were also performed with different numbers of scans by changing the pixel dwell time and the exposure time of the implant appropriately. After FIB implantation, all wafers were heat-treated by rapid thermal annealing at 600°C or 700°C for 30 s in N$_2$ to obtain the solid state regrowth of the implanted Si layer and to anneal the damage caused by ion implantation.

$I$–$V$ and $C$–$V$ characteristics of the diodes were measured using an HP 4140B pA meter and an HP 4820 C–$V$ meter. The temperature of these measurements was varied from 25 to 200°C to determine the dominant mechanism (i.e., diffusion, generation, or tunneling) contributing to junction leakage current.

The junction depths for the diodes fabricated on the N$_b$ substrate were measured by the spreading resistance profiling (SRP) technique and have been reported earlier [7]. Fig. 1 shows the depth profiles measured by secondary ion mass spectroscopy (SIMS) and SRP techniques on N$_b$ substrates in order to estimate the atomic and carrier concentration profiles, the peak concentration depth ($R_p$), and the junction depth ($x_j$) of 15 keV /$1 \times 10^{15}$ cm$^{-3}$ FIB implantation. An $R_p$ and $x_j$ of approximately 15 and 78 nm, respectively, are obtained from the as-implanted SIMS and SRP profiles. $R_p$ as shallow as 2.5 nm [8] for a 2 keV Ga implantation and an $x_j$ of 17 nm for 4 keV [7] implant have been previously obtained. A systematic study of the dependence of $x_j$ versus implanted Ga energy indicated a nearly linear relationship [7]. Although attempts to measure $x_j$ for implanted energies less than 4 keV proved unsuccessful due to the limitations of the SRP technique, we expect the junction depths for these cases to be between 8 and 14 nm. Based upon the values of $x_j$ obtained for implants on N$_b$ substrates, the corresponding depths of the junctions fabricated on the N$_b$ substrates are expected to be much shallower.

The value of carrier concentration in Fig. 1 measured by SRP is calculated by assuming an effective value for the hole mobility of B-doped Si, since the hole mobility in shallow layers obtained by low energy Ga implantation is not known. However, the hole mobility of Ga-doped Si has been shown [9], [10] to be at least a factor of 10 times less than that for B-doped Si. Hence, the true carrier concentration is realistically expected to be an order of magnitude higher than indicated in Fig. 1. This conclusion has been experimentally tested by performing a series of electrochemical $C$–$V$ (ECV) measurements of samples implanted with low energy FIB Ga. The ECV profiles indicate carrier concentration well in the excess of $10^{19}$ cm$^{-3}$ [11].

III. RESULTS AND DISCUSSION

The effect of substrate concentration on diodes fabricated using FIB Ga implantation under different conditions but with a constant dose of $1 \times 10^{15}$ cm$^{-2}$ and common annealing conditions of 600°C for 30 s has been investigated. The $I$–$V$ characteristics of those diodes are shown in Fig. 2. Salient features evident from the figure are: 1) comparison of the 10 keV diodes at $-5$ V bias indicates that the diode fabricated on the N$_b$ substrate has a leakage current 100× smaller than the diode fabricated on the N$_b$ substrate; 2) the leakage current for the N$_b$ diode exhibits a strong dependence on the applied voltage (especially with $V_h > 4$ V), while the N$_b$ diode is fairly immune to the applied reverse bias; and 3) comparison of the N$_b$ diodes indicates a leakage current approximately 100–500× smaller for the 10 keV versus the 50 keV diode. The results of Fig. 2 indicate the tunneling effect on the leakage current for diodes fabricated on N$_b$, due to the high background concentration. The reverse breakdown voltages for the diodes fabricated on the N$_b$ substrates ranged between 100 and 110 V, whereas for the diodes on N$_b$ substrates, the breakdown voltage was measured to be between 12 and 16 V. Evidence of tunneling can be obtained from the temperature dependence of the $I$–$V$ measurements. Fig. 3 shows the temperature dependence of the junction leakage current for a 10 keV /$10^{15}$ cm$^{-3}$ diode fabricated on N$_b$ substrate. It is observed that the leakage current shows a weak temperature dependence which is consistent with the fact that tunneling current ($I_{tunnel}$) is relatively insensitive to temperature [12]. Under forward bias, tunneling can also lead to an anomalously high, nonideal current for dopant concentrations greater than $10^{18}$ cm$^{-3}$ [3]. The tunneling current could be either phonon-assisted or trap-assisted and is also relatively insensitive to temperature. Fig. 4 shows the effect of tem-
temperature on the forward bias current \( I_F \) at a fixed bias \( V_F = 0.6 \) V. For the diode fabricated on \( N_s \) substrate, \( I_F \) increases only slightly between 25 and 100°C. However, a much more rapid increase in \( I_F \) is observed as the temperature is increased beyond 100°C. We interpret this behavior to mean that the tunneling mechanism dominates the forward current up to 100°C, while for higher temperatures diffusion and generation mechanisms are dominant. This relation of the forward current versus temperature is consistent with a tunneling current behavior as shown in [12] and [13]. In contrast, for the \( N_s \) substrate, the forward current increased rapidly from 25°C, indicating the absence of tunneling. The temperature dependence of a 10 keV/10^{15} \text{ cm}^{-2} \) diode fabricated on \( N_s \) substrate is shown in Fig. 5. In this case, \( I_F \) shows a strong temperature dependence, indicating that transport is dominated by diffusion and generation mechanisms.

To determine the contribution of diffusion and generation currents to the overall leakage, the log of \( I_F \) for the \( N_s \) and \( N_s^+ \) diodes annealed at 600°C is plotted as a function of the inverse of temperature in Fig. 6 for a fixed \( V_R \) of 2 V, where tunneling is not dominant in \( N_s^+ \) diodes. The generation current component is dominant up to 91°C and 106°C for the diodes fabricated on \( N_s \) and \( N_s^+ \) substrates, respectively. Both these values compare favorably to B-implanted diodes annealed at 1000°C, which have been reported [14] to have generation current domination up to 110°C.

Fig. 7(a) shows the energy dependence of the leakage current at -5 V for diodes fabricated with different doses and substrate concentrations. Diodes with very low leakage currents can be fabricated on \( N_s \) substrates with implant energy as low as 2 keV, indicating the absence of residual damage in the depletion region. For \( N_s \) substrates, the leakage current does not vary significantly...
consistent with previously published results [2] for BF$_{2}$ implantation, where a 5 keV implant was observed to result in smaller tunneling current than a 15 keV implant. Another reason for the difference in the leakage currents for the two substrates is related to the fact that in the N$_{b}$ substrate, the p–n junction depletion layer region lies much deeper than in the N$_{c}$ substrate. Therefore, fewer implantation-induced defects will be incorporated into the depletion layer region for the N$_{b}$ substrate as compared to the N$_{c}$ substrate.

It is expected with the scaling of future CMOS VLSI devices that the power supply required for these submicron devices will scale accordingly. Analytical expressions relating the power supply voltage and the device design rules have been obtained and experimentally tested [16]. Based upon these relations, we expect the choice of power supply for junctions such as those reported in this paper to be approximately 1.3 V. The values of $I_{R}$ at 1.3 V for junctions fabricated in the N$_{c}$ substrates at different implantation energies with a dose of 10$^{13}$ cm$^{-2}$ are also included in Fig. 7(a). The data indicate that the reduction in power supply from 5 to 1.3 V will result in an order of magnitude reduction in leakage current. For example, for diodes implanted with 15 keV Ga$^{+}$ result in $I_{R}$ (1.3 V) = 2 × 10$^{-10}$ A, while $I_{R}$ (5 V) = 3 × 10$^{-9}$ A. This represents an acceptable set of conditions for future CMOS p–n junctions characteristics: heavily doped (10$^{18}$ cm$^{-3}$) substrate, shallow junction depth (15–20 nm for 15 keV Ga$^{+}$ implantation), and moderate leakage current density ($\approx$ 60–70 nA/cm$^{2}$).

Fig. 7(b) plots the ideality factors ($n$) obtained from diodes implanted at various energies. It is observed that for the diodes fabricated on the heavily doped substrates, $n$ ranges between 1.5 and 2.5, reflecting the nonideal characteristics indicative of the tunneling mechanism [3]; whereas for the diodes fabricated in N$_{b}$ substrates, values of $n$ are very close to 1.

Fig. 8 shows the I–V profiles for diodes fabricated with an implant energy of 15 keV at doses varying from 1 × 10$^{13}$ to 1 × 10$^{15}$ cm$^{-2}$ on the N$_{c}$ substrate. As the dose is increased from 1 × 10$^{13}$ to 5 × 10$^{13}$ cm$^{-2}$, a decrease in leakage current of 10$^{15}$–10$^{14}$ is obtained depending on the value of the reverse bias. Fig. 9 summarizes the dependence of leakage current (at 5 V reverse bias) on the implanted dose for different Ga implantation energies on N$_{b}$ and N$_{c}$ substrates. The main points observed in Fig. 9 are: 1) for the diodes fabricated at 2 keV on either substrate, the leakage current decreases monotonically with increasing dose; 2) at 5 keV, diodes fabricated on the N$_{b}$ substrate show only a negligible amount of dose dependence; 3) diodes fabricated on the N$_{c}$ substrate with 5–15 keV Ga$^{+}$ implantation show an increase in leakage current as the dose increases from 5 × 10$^{13}$ to 1 × 10$^{14}$ cm$^{-2}$. However, a further increase in the dose (1 × 10$^{15}$ cm$^{-2}$) is accompanied by a decrease in leakage current. For example, for implantation with 15 keV Ga$^{+}$, the $I_{R}$ for the 1 × 10$^{14}$ cm$^{-2}$ dose is approximately 20× larger than the $I_{R}$ for a 5 × 10$^{13}$ cm$^{-2}$. Upon increasing the dose
to $1 \times 10^{15}$ cm$^{-2}$, it is observed that the $I_P$ decreases by
150$\times$ over the value obtained for $1 \times 10^{14}$ cm$^{-2}$.

In order to study the effect of scan speed on the electrical characteristics, diodes were also fabricated with 5–15 keV/1 $\times$ 10$^{15}$ cm$^{-2}$ on an $N_a$ substrate using multiple scans (MS) by changing the dwell time of the implant. The net effect of multiple scans is to change the implantation dose rate. Using MS FIB implantation, defects are not generated continuously at any one location [17], and thus may have enough time to self-anneal to a certain extent until the next scan. In the case of single-scan (SS) FIB implantation, each pixel receives the entire dose continuously with a much-reduced opportunity to self-anneal, thus possibly leading to a higher final damage level. Fig. 10 compares the effect of multiple scans on the $I-V$ characteristics. The data indicate that for reverse bias voltages greater than 5 V, there is no apparent scan speed dependence. At reverse bias <5 V, a change in the leakage current is observed with respect to the scan speed. This could be due to the fact that at lower reverse bias, the depletion width region lies closer to the edge of the implanted region. For most cases, it was observed that the leakage current of MS diodes is lower than that of SS diodes. Fig. 10 also shows that as the implant energy increases from 5 to 15 keV, the forward characteristics of the $N_a$ diodes become insensitive to the effect of multiple scans. Multiple scan implantations on the $N_a$ substrate resulted in diode $I-V$ characteristics which showed only a very small scan speed dependence as compared to the $N_a$ samples. In general, it is interesting to note that while the number of implant scans are changed significantly, there is not an appreciable difference in the $I-V$ characteristics of the FIB fabricated diodes.

$I-V$ measurements were performed on diodes annealed at two different temperatures to observe the dependence of leakage current on anneal temperature. Fig. 11 compares the $I-V$ characteristic of diodes fabricated on a $N_a$ substrate with 10 keV/1 $\times$ 10$^{15}$ cm$^{-2}$ Ga implant and annealed at 600°C and at 700°C for 30 s. The figure shows that the diode annealed at 700°C is approximately 1000$\times$ leakier than the diode annealed at 600°C. This effect can be attributed to a "reverse anneal," namely, a decrease in the electrical activity of the implanted ions when a certain critical anneal temperature is exceeded. This effect is consistent with the fact that Ga atoms implanted into Si are known to precipitate easily and form
electricaly inactive clusters when annealed at higher temperatures (exceeding 600°C) [18], [19]. This behavior was also exhibited by diodes fabricated at 5 and 15 keV, with the leakage current at -5 V for diodes annealed at 600°C being 100-200 × smaller than the corresponding diodes annealed at 700°C.

Finally, Fig. 12 shows the capacitance-voltage (C-V) measurements made for diodes fabricated on the two different substrates. As expected under reverse bias, the values of capacitance for the lightly doped substrate are significantly lower than the corresponding values for the Nb substrate. The abrupt nature of these junctions was confirmed by plotting C' versus V, which yielded a straight line as shown in the inset of Fig. 12.

IV. CONCLUSIONS

A systematic study of energy and dose dependence of FIB Ga^+ implanted shallow junctions on Si substrates with a range of background concentrations has been performed. The results indicate that for Nb substrates an optimal implantation condition with regard to the electrical properties exists at 15 keV / 1 × 10^{15} cm^{-2}, while for N_p substrates, the I-V characteristics were found to be relatively insensitive to implant energy. The tunneling component of the leakage current dominated the electrical properties of the diodes fabricated on the N_p substrates. A major reason for the difference in the electrical properties between diodes on the two different substrates could arise from the location of defects with respect to the diode depletion region. An RTA anneal of 600°C / 30 s was determined to provide reduced leakage currents.

REFERENCES

Homyar C. Mogul is currently a Ph.D. student in the Department of Electrical Engineering at the University of Cincinnati working under the supervision of Dr. Andrew J. Steckl. His research involves using Ga-based focused ion beam (FIB) implantation technology for application in fabrication of sub-quarter micron CMOS technology. His research interests include processing, fabrication and testing of sub-micron devices, silicon technology, characterization, sub-micron lithography, materials processing, flat-panel display devices, Si-based optoelectronics technology, and exploratory structures/devices.

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