Electrical properties of nanometer-scale Si p^+-n junctions fabricated by low energy Ga^+ focused ion beam implantation

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Diodes have been fabricated by on-axis Ga^+ focused ion beam (FIB) implantation at 4–25 keV into n-Si ⟨100⟩ wafers doped to $2\times10^{15}/cm^3$. Post-implantation anneal was performed at 600 °C for 30 s to electrically activate the Ga and to regrow the implanted layer. SIMS measurements performed to obtain the Ga concentration depth profile indicate good agreement with TRIM simulation even at low energies. At 4 keV an electrical junction depth of 15 nm is obtained from spreading resistance profiling (SRP). The junction depth was found to vary linearly with energy over the range explored. The electrical properties of the diodes were obtained from I-V characteristics. The leakage current density of the 5 keV diode was measured to be 1 and 20 nA/cm^2 at a reverse bias of 1 and 5 V, respectively. The corresponding leakage current density values for the 10 and 15 keV diodes were between 25% and 50% lower than those reported for 5 keV. The reverse bias breakdown voltage was between 105 and 110 V for all diodes. The combination of nanometer-scale junction depth, low leakage current density, and high breakdown voltage indicate that low energy Ga FIB implantation is a promising technology for ultrashallow p^+-n junction fabrication.

I. INTRODUCTION

Future CMOS technology will require p^+-n junctions with depths considerably less than 0.1 μm.[1] To achieve this goal various diffusion- and implantation-based techniques are being pursued.[2] Among the attractive implantation-based approaches is the use of heavy mass column III ions which have shallow penetration depths. Conventional (i.e., broad beam) implantation of Ga^+ has been reported[3] to result in sub-100 nm p-n junctions. Ga is an effective amorphizing species resulting in only minor channeling under most implantation conditions. The amorphized Si layer can be recrystallized by rapid thermal annealing at low temperatures and thus minimizing diffusion effects. Since Ga has a low equilibrium solid solubility in Si and high diffusivity through SiO_2 it should be utilized only in those elements of the integrated circuit where junction depth is paramount. To provide this flexibility, the use of focused ion beam implantation[4] with its maskless, resistless process is advantageous. FIB Ga^+ implantation, at energies ranging primarily from 50 to 75 keV, has been shown[5] to produce 200–220 nm shallow junctions with low (24 nA/cm^2) leakage current. Recently, the use of low energy (5–15 keV) Ga^+ FIB implantation has been reported[6] to yield junction depths as shallow as 20 nm. While this previous paper[6] discussed the FIB implantation process and the materials (structure, composition) properties, in this paper we report on some of the electrical properties of these nanometer-scale p^+-n junctions.

II. EXPERIMENTAL CONDITIONS

Si wafers with ⟨100⟩ orientation and background doping (phosphorus) concentration of $(1–2)\times10^{15}$ cm^{-3} were employed for the fabrication of samples for both materials analysis and electrical measurements.[6] Sample fabrication for electrical characterization used a two mask process in conjunction with Al liftoff for the contacts. The Al was sintered after liftoff at 300 °C for 9 min to improve the electrical contact, while avoiding Al spiking.

The Ga^+ ion implantation was performed perpendicular to the substrates using a MicroBeam, Inc. NanoFab 150 system. The operation of the NanoFab 150 for the purpose of shallow junction fabrication was previously described.[6] While in general much higher beam current density is available in FIB implantation, as opposed to the BB case, for the low energy FIB implants the current density was similar to that of conventional implanter, 25–50 mA/cm^2. This has the advantage of eliminating FIB dose rate effects possibly present at the higher FIB current density.

The experiments were carried out with a Ga liquid metal ion source containing the natural distribution of isotopes and ionized species.[6] Single serpentine scan was used to provide a dose of 1×10^{15} cm^{-2}. After FIB implantation, all wafers were heat treated by rapid thermal annealing at 600 °C for 30 s in N_2 to obtain the solid state regrowth of the material and to anneal the damage caused by ion implantation.

Companion samples were prepared under similar processing and implantation conditions for materials analysis. Secondary ion mass spectroscopy (SIMS) and spreading resistance profiling (SRP) were performed to obtain the atomic gallium and carrier concentration depth profiles and junction depths resulting from the annealing condition. Cross-sectional TEM was performed to obtain information about the damage due to implantation in the Si substrate before and after RTA annealing. In the case of the diodes, I-V and C-V characteristics were measured using a HP 4140B pA meter and a HP 4820 C-V meter. All electrical measurements were performed at room temperature.

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III. EXPERIMENTAL RESULTS

In this paper, we concentrate on the electrical properties of the FIB implanted nanojunctions. The electrical characterization methods used are *I-V* and *C-V* measurements. Secondary ion mass spectroscopy (SIMS), spreading resistance profiling (SRP) and cross-sectional TEM (*x*-TEM) were performed as a part of materials characterization and a detailed explanation of these results have been published elsewhere.[6]

Figure 1 shows the profiles of atomic Ga and resulting hole concentration versus depth for the 5-keV Ga FIB implant into Si (100). The profile in the upper half of the figure was measured using SIMS with a 1 kV Cs^+ beam at a 60° impact angle, to minimize the effects due to ion beam mixing that can result in a erroneous depth profile. Superimposed on this experimental profile is a simulated TRIM[7] profile for 5-keV Ga implantation into Si assuming an amorphous target. The experimentally obtained profile is about 2 nm shallower than the profile predicted by TRIM. This could be due to the fact that the initial sputter rate during SIMS measurement is much faster than the steady state sputter rate. A minor exponential "tail" was observed in the case of the experimental profile indicating that some channeling occurred during implantation into crystalline Si. The lower half of Fig. 1 is a corresponding SRP profile of the 5-keV Ga FIB implant into Si (100) indicating the location of the electrical

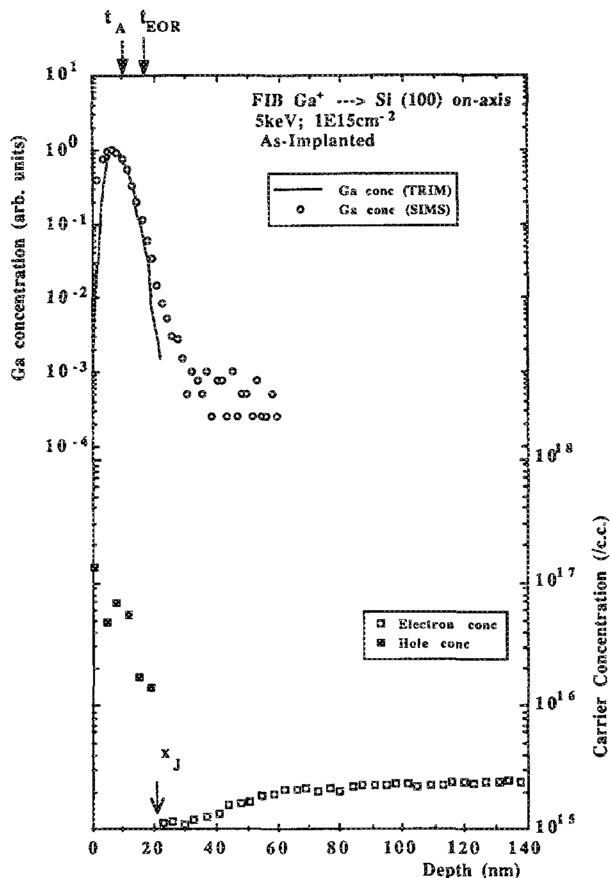

FIG. 1. Atomic Ga and carrier concentration vs depth for 5 kV implantation.

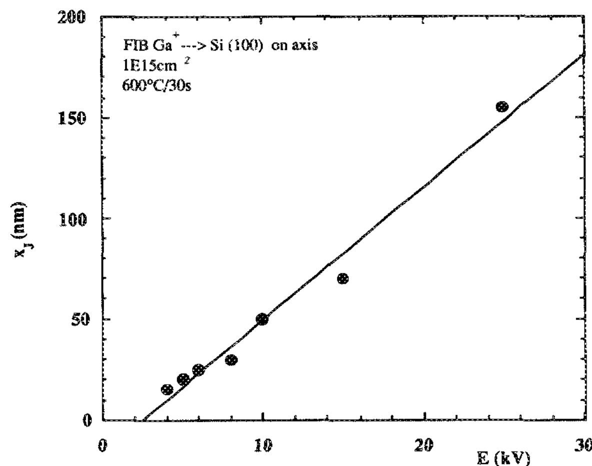

FIG. 2. Junction depth vs Ga^+ implantation energy.

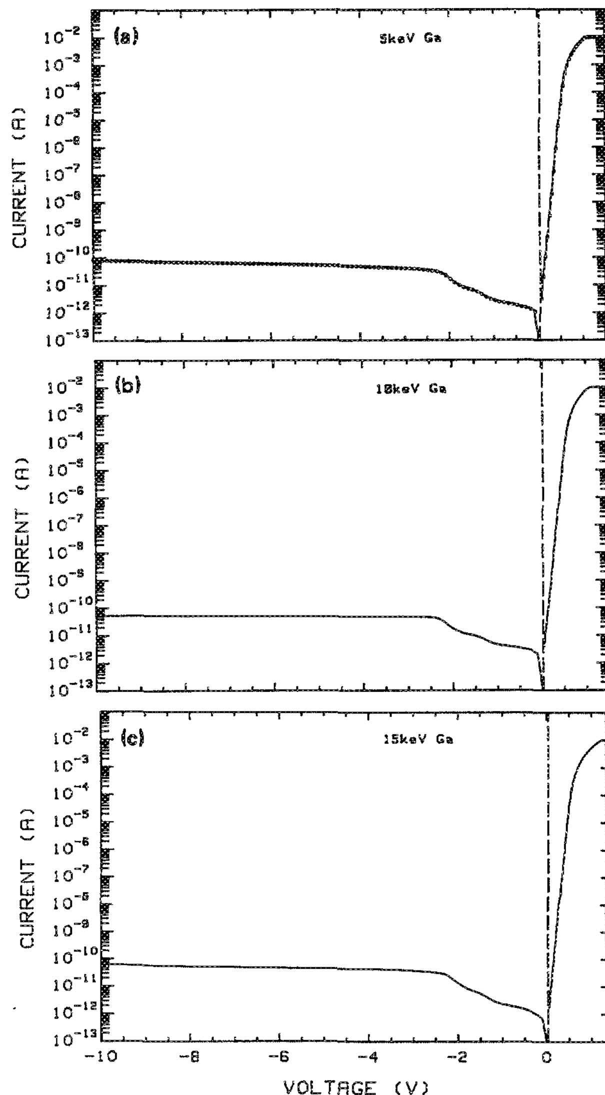

FIG. 3. *I-V* characteristics for Ga-implanted diodes: (a) 5, (b) 10, (c) 15 kV.

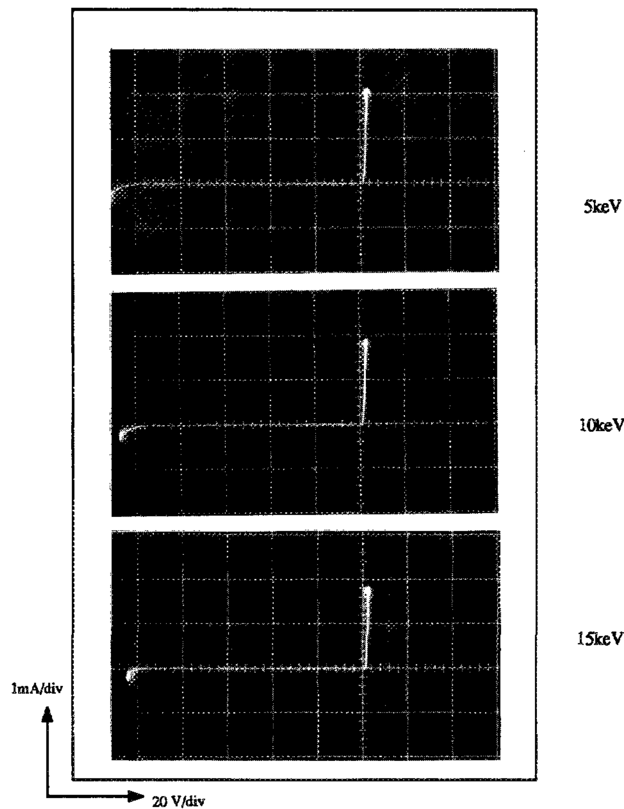

FIG. 4. I-V characteristics of Ga-implanted diodes indicating breakdown voltage.

junction to be approximately 20 nm below the surface of the substrate. This result is in good agreement with our x-TEM result[6] which shows that the location of the end-of-the-range damage, t_{EOR}, to be around 20 nm from the substrate surface. It should also be noted that the value of the carrier concentration obtained from SRP would be significantly higher if the mobility of Ga-implanted Si were to be taken into account.[8]

SRP measurements were also performed on samples with different implantation energies, ranging from 4 to 25 keV. Figure 2 shows the dependence of the location of the junction depth as a function of the implanted Ga energy. Although SRP measures a wide range of resistivity, there are unfortunately a number of factors that limit this technique's usefulness, especially while profiling such shallow junctions as reported in this study. Some of the more serious limitations of this technique include carrier spilling, effective mobility, shallow angle bevels which affect the carrier distribution and can cause a distortion of the implant profiles, and crystalline imperfections which can lead to noise problems due to small sampling volume. The linearity of Fig. 2 does ascertain the fact the values for junction depth obtained in our case are probably fairly accurate.

To evaluate the electrical quality of the p^+-n diodes, I-V characteristics of junctions with an area of $540\times540\ \mu\mathrm{m}^2$ FIB Ga^+ implanted at 5, 10, and 15 keV with a dose of $1\times10^{15}/\mathrm{cm}^2$, were measured under both forward and reverse bias. The results of these measurements are shown in Fig. 3. For these diodes a current density (J_R) of 15–20 $\mathrm{nA/cm}^2$ was measured at 5 V reverse bias and an ideality factor (n), of 1.02–1.06 (measured from 10^{-12} to 10^{-5} A) was obtained in forward bias.

In general, the Ga-implanted diodes have excellent breakdown voltages ranging from 100–110 V. As shown in Fig. 4, no significant difference in the breakdown voltage is observed between the diodes fabricated with different implantation energies. A summary of J_R values at -10, -5, and

TABLE I. Summary of electrical characteristics of Ga^+ FIB-implanted diodes. Area $=540\times540\ \mu\mathrm{m}^2$

E (keV)	J_R (-10 V) nA/cm^2	J_R (-5 V) nA/cm^2	J_R (-1 V) nA/cm^2	n	V_{BR} (V)
5	31.62	20.4	0.9	1.059	≈115
10	17.8	15.5	0.7	1.026	≈108
15	17.7	16.3	0.6	1.026	≈104

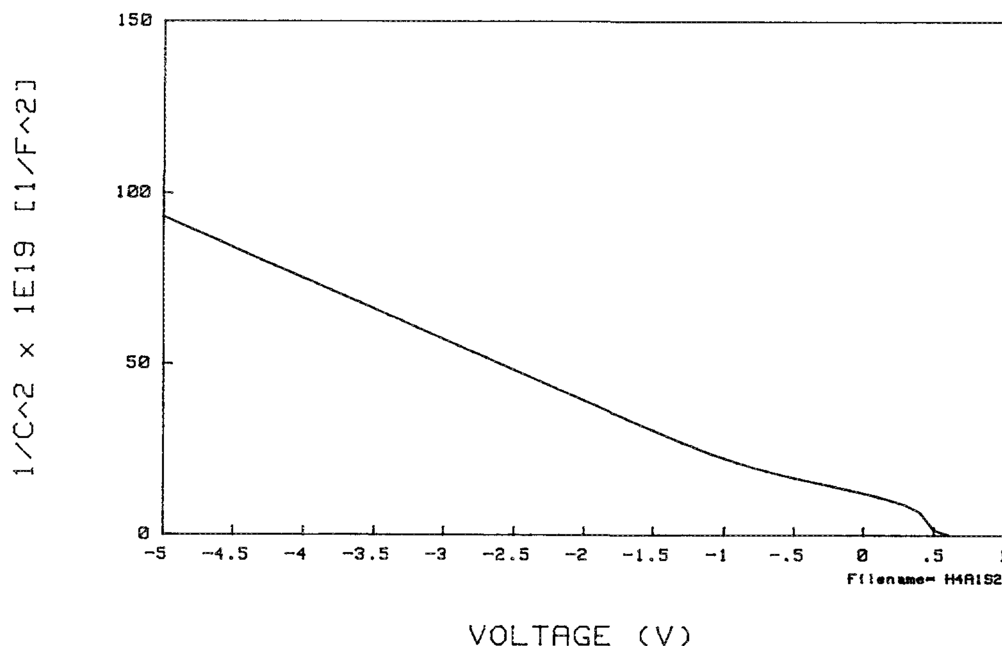

FIG. 5. C-V characteristics for 10 kV Ga-implanted diode.

-1 V along with the ideality factor and the breakdown voltage are shown in Table I for each implantation energy.

The abrupt nature of the Ga-implanted shallow junctions as seen via the SRP profile in Fig. 1 can be further confirmed by *C-V* measurement. Figure 5 shows the $1/C^2$ versus voltage behavior measured by biasing the 10 keV Ga-implanted diode from -5 V (reverse bias) to 1 V (forward bias). A nearly straight line is observed indicating that the junction is fairly abrupt.

IV. CONCLUSIONS

Low energy Ga was implanted into crystalline Si with the intent of fabricating nanoscale, damage-free, device-grade diodes. Ga implanted diodes with junction depth as shallow as 15 nm have been obtained by low thermal budget post-implantation processing. Our investigations indicate that this Ga-based, low-temperature process can produce the neccessary p^+-n diode characteristics required for submicrometer PMOS/CMOS technology.

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