Sub-100-nm p^+-n shallow junctions fabricated by group III dual ion implantation and rapid thermal annealing

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The fabrication of p^+-n junctions with depth less than 100 nm using dual ion implantation of group III species (^{69}Ga, ^{115}In, ^{11}B, $^{49}BF_2$) in various combinations is reported. We have investigated both the single use of heavy group III (Ga and In) ions for creating shallow junctions and the dual implant approach where Ga or In was first used for preamorphization (and doping) followed by a B or BF_2 implant. The optimum cases for sub-100-nm shallow junction formation among the group III combinations evaluated are Ga/B dual ion implantation followed by low-temperature (550–600 °C) rapid thermal annealing (RTA) for 15–30 s and In/B(B or BF_2) dual ion implantation with higher temperature (900–1000 °C) RTA for 10 s. Junction depths of 60–100 nm and sheet resistances of 150–300 Ω/□ were obtained. Shallow junction diodes fabricated by this dual ion implant technology exhibit low leakage current densities of 8–30 nA/cm^2 and good ideality factors of 1.01–1.05.

Sub-100-nm shallow junction diodes with low sheet resistance and good junction characteristics will be necessary to form the source and drain regions of metal-oxide-semiconductor field-effect transistors (MOSFETs) with channel length in the deep submicron regime.[1] Whereas n^+-p shallow junctions are fairly readily fabricated using As or possibly Sb, p^+-n shallow junctions are considerably more difficult to obtain, normally requiring very low energy B and/or BF_2 implantations preceded by Si or Ge amorphization.[2,3] To obtain good junction characteristics with Si or Ge preamorphization requires high-temperature annealing (1000–1100 °C) in order to remove the preimplant damage, resulting in a deeper junction. It has been reported that the damage created by implantation of group IV ions is greater and more difficult to remove as compared to that of group III ions.[4] Ganin *et al.* have determined[5] that B-implanted p-n junctions preamorphized with In and rapid thermally annealed (RTA) at high temperatures (1150 °C) exhibit near complete removal of extended defects, whereas with Si preamorphization unannealed defects are still present. In addition, highly activated and good quality Ga-implanted p^+-n junctions have been recently obtained with low-temperature (550–600 °C) RTA.[6,7] In this letter, we report on the fabrication of p^+-n junctions with depths less than or approximately equal to 100 nm by using dual ion implantation of group III species (^{69}Ga, ^{115}In, ^{11}B, $^{49}BF_2$) in various combinations. We have investigated both the single use of heavy group III (Ga and In) ions for creating shallow junctions and the dual implant approach where Ga or In was first used for preamorphization (and doping) followed by a B or BF_2 implant. All the implants were performed along the ⟨100⟩ direction, since it has been reported that off-axis implantation results in asymmetric device characteristics for submicron devices.[8,9] RTA has been used throughout to obtain maximum dopant activation and damage removal at minimum thermal budgets.

⟨100⟩ oriented Si wafers with 2.5–3 μm P-doped (5×10^{15}/cm^3) epilayers on Sb-doped n^+ (2×10^{18}/cm^3) substrates were used. For material analysis, monitor wafers were prepared with an 8 nm oxide. Group III dual ion implants in various combinations (Ga/B, Ga/BF_2, In/B, In/BF_2) were performed with different implant energies and doses (25–50 keV and $1–10\times10^{14}$ cm^{-2} for Ga and In implants, 25 keV and $1–2\times10^{15}$ cm^{-2} for BF_2 implant, 3–5 keV and 1×10^{15} cm^{-2} for B implant). The implants were performed at a current density less than 0.8 μA/cm^2 to avoid ion beam heating during implantation. All the wafers were diced into 0.8×0.8 cm^2 chips and subsequently annealed at temperatures between 550 and 1000 °C for 10–60 s. The B-, Ga-, and In-implanted atomic concentration profiles were characterized before and after RTA treatment by secondary-ion mass spectrometry (SIMS). Spreading resistance profiling (SRP) was used to obtain carrier concentration depth profiles and junction depths. The estimated accuracy for SRP data of shallow junctions of $\leqslant$100 nm is $\pm$ 10%. The sheet resistance of the implanted thin layer was measured by the four-point probe (FPP) technique. Rutherford backscattering spectrometry (RBS)/channeling with a 2 MeV He^+ ion beam was used to obtain the implantation damage in the Si substrate before and after annealing. In addition, p^+-n shallow junction diodes with areas ranging from 22×12 to 900×900 μm^2 were fabricated using the group III dual ion implantation technology and a standard dielectric isolation MOSFET process. To replicate the MOSFET process, a punchthrough control implant (P, 90 keV at a dose of 2×10^{12}/cm^2) was performed resulting in a substrate concentration of 1×10^{17}/cm^3 from the Si surface to a depth of 0.4 μm.

The B-, Ga-, and In-implanted atomic concentration

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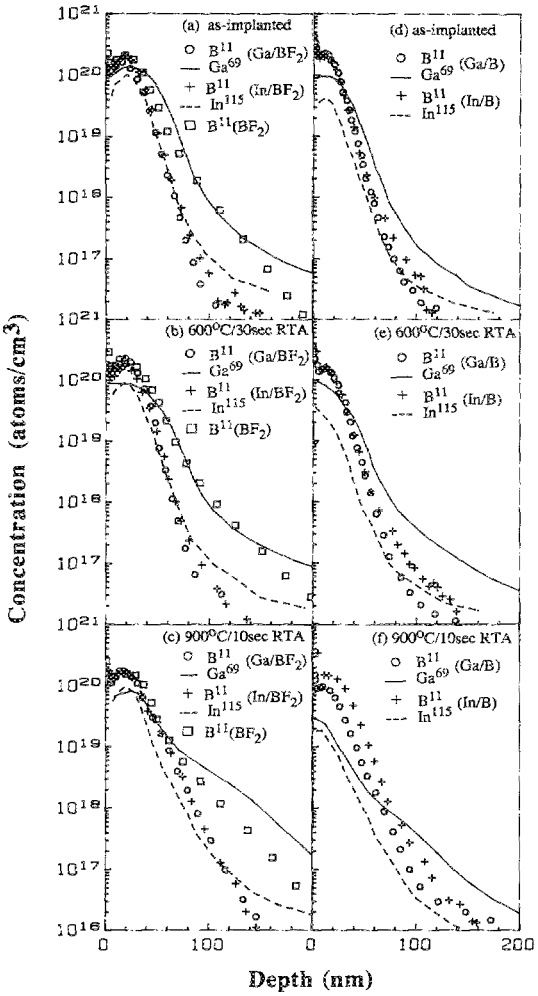

FIG. 1. SIMS depth profiles for as-implanted and annealed samples. Implantation conditions Ga/BF_2 at 50/25 keV, $1\times10^{15}/1\times10^{15}$ cm^{-2}; In/BF_2 at 50/25 keV, $1\times10^{15}/1\times10^{15}$ cm^{-2}; BF_2 at 25 keV, 1×10^{15} cm^{-2}; Ga/B at 25/3 keV, $5\times10^{15}/1\times10^{15}$ cm^{-2}; In/B at 30/3 keV, $1\times10^{14}/1\times10^{15}$ cm^{-2}.

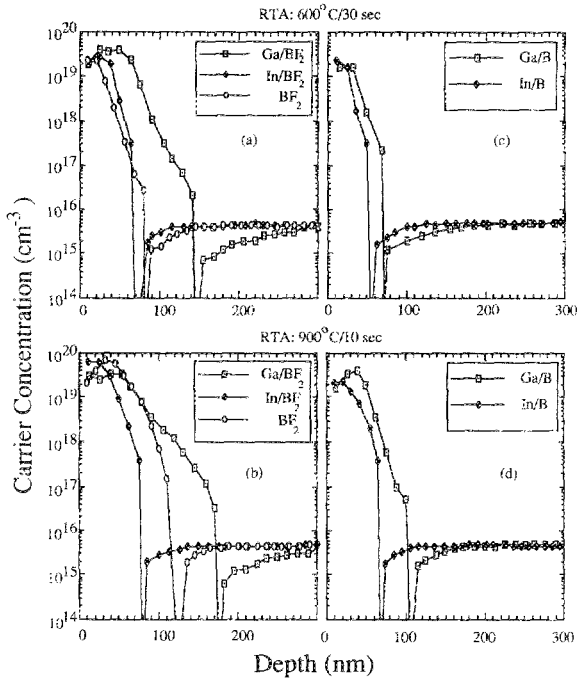

FIG. 2. Carrier concentration (SRP) depth profiles for the annealed samples as in Fig. 1.

profiles of Ga/BF_2 (50/25 keV, $1\times10^{15}/1\times10^{15}$ cm^{-2}) and In/BF_2 (50/25 keV, $3\times10^{14}/1\times10^{15}$ cm^{-2}) are shown in Figs. 1(a), 1(b), and 1(c) for as-implanted, 600 °C/30 s, and 900 °C/10 s annealed samples, respectively. Boron SIMS profiles of BF_2 (25 keV, 1×10^{15} cm^{-2}) single ion implant are also included for comparison. The boron channeling tail is greatly reduced in the dual ion-implanted samples where the Si substrate surface layer was first preamorphized by Ga or In implantation. Therefore, the boron profiles of the dual ion implants are considerably shallower than those of the BF_2-only implant, both before and after annealing. This phenomenon is further confirmed by carrier concentration profiles obtained from SRP measurements and plotted in Fig. 2(a) for 600 °C/30 s anneal and in Fig. 2(b) for 900 °C/10 s anneal. The junction depths of In/BF_2 dual implant and BF_2 single implant annealed at 900 °C are 80 ($\pm$ 8) and 125 ($\pm$ 10) nm, respectively, or a 50% difference. For the case of Ga/BF_2 dual implant, although the boron profile is most abrupt, the Ga ions are activated and contribute carriers which result in a deeper junction. Nevertheless, this problem can be solved by adjusting the energy and dosage of the Ga ion implant. Figures 1(d), 1(e), and 1(f) show the B, Ga, and In atomic concentration profiles of Ga/B (25/3 keV, $5\times10^{14}/1\times10^{15}$ cm^{-2}) and In/B (30/3 keV, $1\times10^{14}/1\times10^{15}$ cm^{-2}) dual implants. The projected range of 30 keV In is shorter and the dosage is smaller than for the 25 keV Ga implant. Therefore, the implant-induced amorphous layer is thinner, leading to a deeper boron atomic concentration profile for the In/B dual implanted sample. However, as in the previous case, the junction depth is greater for the Ga/B dual implanted sample due to Ga activation. Junction depths and sheet resistances of the Ga/B dual implanted samples as shown in Figs. 2(c) and 2(d) are 70 ($\pm$ 7) nm and 290 Ω/□ for the 600 °C/30 s anneal and 105 nm and 186 Ω/□ for the 900 °C/10 s anneal. For In/B dual implanted samples, the corresponding values are 55 ($\pm$ 5) nm [see Figs. 2(c) and 2(d)] and 315 Ω/□ for the 600 °C/30 s anneal and 65 ($\pm$ 6) nm and 339 Ω/□ for the 900 °C/10 s anneal.

Various combinations of the group III dual implantation were investigated by changing the energy and dosage. Junction depths and sheet resistances for these experiments, annealed under various temperature/time conditions, are listed in Table I. p^+-n junction depth values as shallow as 55–70 nm have been obtained with 25/3 keV Ga/B, 30/3 keV In/B, 50/5 keV In/B, and 50/25 keV In/BF_2 dual implants. Although highly activated shallow junctions can be obtained by single Ga implantation, the sheet resistance of the implanted thin layer can be further improved by dual implantation, especially for ultrashallow junctions (<70 nm). A comparison of the dual (25/3 keV Ga/B) and single (25 keV Ga) implantations indicates that a much lower sheet resistance was obtained for the dual implanted samples (290 Ω/□ versus 1420 Ω/□), due to boron ions activated through the solid phase epitaxial regrowth process.

Junction characteristics such as leakage current density, ideality factor, and breakdown voltage of the p^+-n diodes have been measured on the implanted junctions with areas of

TABLE I. Sheet resistance, junction depth, and leakage current density (at 5 V reverse bias) of junctions fabricated using single/dual ion implantation.

Species	Implant energy (keV)	Dose ($\times 10^{15}$/cm^2)	Anneal temp/time (°C/s)	Sheet resistance ($\Omega/\square$)	Junction depth (nm)	Leakage current (nA/cm^2)
Ga	25	1	600/30	1420	60	1.76
	50	1	600/30	505	130	1.23
			900/10	555	170	12.34
Ga + B	25/3	0.5/1	600/30	290	70	32.5
			900/10	186	105	...
	50/5	1/1	600/30	191	120	...
			900/10	204	135	...
Ga + BF_2	50/25	1/1	600/30	288	140	123.0
			900/10	262	165	4.2
In + B	30/3	0.1/1	600/30	315	55	830.0
			900/10	339	65	8.09
			1000/10	187	100	...
	50/5	0.3/1	600/30	216	70	123.0
			900/10	213	70	12.3
			1000/10	145	105	...
In + BF_2	50/25	0.3/1	600/30	317	65	...
			900/10	278	80	...
BF_2	25	1	600/30	416	85	...
			900/10	218	125	...

$900\times900\ \mu m^2$. *I-V* characteristics of two representative diodes fabricated with Ga/B and In/B are shown in Fig. 3. The leakage current density for selected implantation cases is shown in Table I. With junction depths of 60–70 nm, the 50/5 keV and 30/3 keV In/B dual implanted and 900 °C/10 s annealed diodes exhibited reverse-bias (at -5 V) leakage current densities and ideality factors of 8–12 nA/cm^2 and 1.01–1.03. For the 25/3 keV Ga/B dual implanted diodes annealed at 600 °C/30 s, corresponding values of 32 nA/cm^2 and 1.03 are obtained. Breakdown voltages of these diodes are 18–20 V. From RBS/channeling measurements of selected samples using the glancing angle technique, as shown in Fig. 3, it was observed that the implantation damage in the Si substrate was well removed through the solid phase epitaxial regrowth process during the annealing step. The oxygen peak observed in the RBS measurements was due to the thin (7–8 nm) silicon dioxide layer covering the Si substrate.

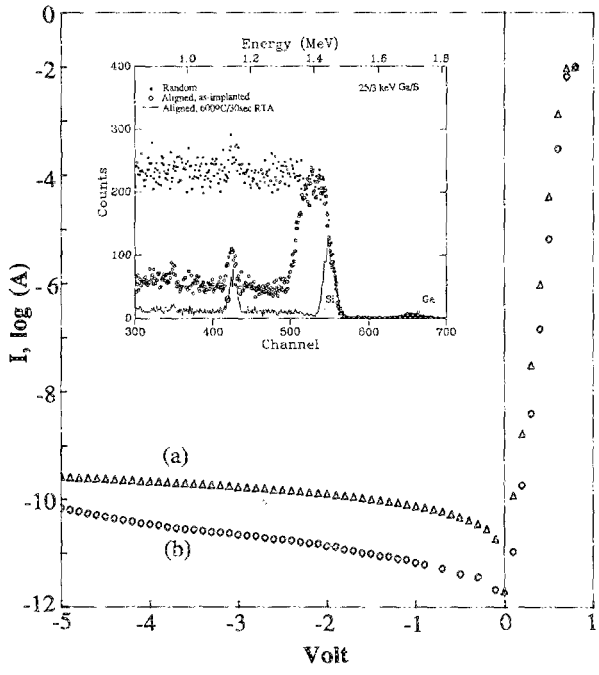

FIG. 3. *p-n* junction current-voltage characteristics: (a) diode implanted with Ga/B at 25/3 keV and $5\times10^{14}/1\times10^{15}$ cm^{-2}, RTA annealed at 600 °C for 30 s; and (b) diode implanted with In/B at 30/3 keV and $1\times10^{14}/1\times10^{15}$ cm^{-2}, RTA annealed at 900 °C for 10 s. Inset: RBS/channeling spectra for diode in (a) above.

In summary, we have shown that in using all group III dual ion implantation, a useful sub-100-nm shallow junction technology has been developed.

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