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Electrical Properties of Ga-Implanted Si p^+-n Shallow Junctions Fabricated by Low-Temperature Rapid Thermal Annealing

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Abstract—**p^+-n shallow junction diodes were fabricated using on-axis Ga^{69} implantation into crystalline and preamorphized Si, at energies of 25-75 keV for a dose of $1 \times 10^{15}/cm^2$, in excess of the dosage ($2 \times 10^{14}/cm^2$) required to render the implanted layer amorphous. Rapid thermal annealing at 550-600°C for 30 s resulted in the solid phase epitaxial (SPE) regrowth of the implanted region accompanied by high Ga activation and shallow junction formation, 60-130 nm. Good diode electrical characteristics for the Ga implantation into crystalline Si were obtained: leakage current density of 1-1.5 nA/cm² and ideality factor of 1.01-1.03. Ga implantation into preamorphized Si resulted in a two to three times decrease in sheet resistance but a leakage current density orders of magnitude higher.**

I. Introduction

SHALLOW junctions with low sheet resistance are required to form the source and drain regions of short-channel MOSFET's [1]. As FET's are scaled down further into the deep submicrometer regime, junction depths of 100 nm or less are being investigated for both n^+-p [2] and p^+-n [3] technology. This requirement is especially difficult to fulfill for PMOSFET's, which are normally obtained by B^{11} or BF_2^{49} implantation, due to the longer projection range and higher diffusivity of boron as compared to As and Sb, which are generally used in the fabrication of NMOSFET's [4]. Therefore, to obtain shallow junctions using either B or BF_2 it appears necessary to use very low-energy (1-2 keV B^+) implantation and small time-temperature product annealing. However, such low-energy implantation suffers from very low extraction current and increased channeling effect [5]. In addition, low-temperature anneal (550-600°C) is not sufficient to completely activate the implanted B concentration and to remove the implantation damage. If preamorphization is used to prevent B channeling, damage removal still requires high-temperature annealing even though dopant activation can take place at lower temperatures. Recently, it has been reported that highly activated 100-nm shallow junctions can be obtained by on-axis [6] and off-axis [7], [8] Ga^{69} implantation followed by annealing at 550-600°C for a few tens of seconds via solid phase epitaxial (SPE) regrowth. Low-temperature annealing is sufficient in the case of Ga implantation since the critical dose for amorphization ($2 \times 10^{14}/cm^2$) is lower than the dose normally required for source/drain ($1-3 \times 10^{15}/cm^2$) doping. With this low-temperature annealing process (550-600°C), the problem with Ga fast diffusivity in SiO_2 is avoided without the need for applying a mask layer to prevent Ga ions from implanting into SiO_2 and then diffusing into the Si substrate. In this paper, we discuss the electrical characteristics of the Ga-implanted p^+-n diodes, such as junction leakage current density J_R, ideality factor n, and breakdown voltage V_{BR}, which have not been previously reported.

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II. Experimental

(100)-oriented Si wafers with 2.5-3-μm P-doped ($5 \times 10^{15}/cm^3$) epilayers on Sb-doped n^+ ($2 \times 10^{18}/cm^3$) substrates were used. Electron-beam lithography was used to fabricate diodes with different areas ranging from 22×12 to 900×900 μm^2. After 1-μm-deep registration marks for electron-beam lithography were formed by reactive ion etching into the Si substrate, an 8-nm SiO_2 layer was thermally grown and the diode areas were patterned using positive photoresist as a mask for implantation. Ga implantations were performed on-axis at 25-75 keV for a dose of $1 \times 10^{15}/cm^2$ with a low current density at 0.8 mA/cm² to avoid ion-beam annealing during implantation. Some of the wafers were preamorphized by Si self-implantation (80 keV, $2 \times 10^{15}/cm^2$, 7° off-axis) in order to compare with the Ga-only case. After implantation, a 300-nm CVD oxide was deposited at 400°C for 8 min as passivation for the devices. All device wafers were subsequently heat treated by RTA using an A.G. Associates Heatpulse 410 system at 600°C for 30 s. Some of these wafers were then further RTA annealed at 900°C for 10 s. Contact windows were then opened and Al-1-percent Si was evaporated for metallization and patterned. A low-temperature sintering step at 300°C for 15 min in a nitrogen ambient was used to improve the ohmic contact while avoiding aluminum spiking.

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In addition, monitor wafers were similarly processed for material analysis only. Secondary ion mass spectrometry (SIMS) and spreading resistance profiling (SRP) were performed on the monitor wafers to obtain gallium and carrier concentration depth profiles and junction depths resulting from various implantation and annealing conditions. The sheet resistance of the implanted thin layer was measured by the four-point-probe (FPP) technique. Rutherford backscattering spectrometry (RBS) was used to obtain the implantation damage in the Si substrate before and after RTA annealing. For the diodes, $I-V$ and $C-V$ characteristics were measured using an HP 4140B pA meter and an HP 4280 $C-V$ meter. Deep-level transient spectrometry (DLTS) measurements were performed to detect deep levels resulting from implantation damage. $I-V$ characteristics were also measured in the temperature regime ranging from 10 to 125°C using a Keithley logarithmic picoammeter to determine the dominant mechanism (1-kT diffusion or 2-kT generation) contributing to the reverse-bias junction leakage current.

III. Results and Discussions

Fig. 1 shows the SIMS profiles of 50-keV Ga implantation including both as-implanted and RTA-annealed samples at 550 and 900°C. The as-implanted profile for Ga implantation into preamorphized silicon is also included for comparison. Since the implantations were performed on-axially, the channeling distribution tail is observed. However, from the SRP analysis, we have verified that this tail was not fully activated during 550–600°C RTA anneals. Therefore, junction depths of 110–130 nm are obtained, which is close to the 100–120 nm values measured for the preamorphized case. The abrupt nature of the junction was further confirmed by $C-V$ measurements of these p^+-n diodes. For the 900°C anneal, substantial Ga diffusion is observed resulting in a junction depth of 170 nm. A kink at the original amorphous-crystalline (α–c) interface is seen in the corresponding SIMS profile in Fig. 1. As reported by Harrison *et al.* [7], this phenomenon may imply that gallium ions precipitate in the silicon substrate at the end-of-range damage region.

The junction depth and sheet resistance for Ga implantation at different energies are shown in Fig. 2 as a function of anneal temperature. The shallowest junctions of 60 nm were obtained for 25-keV Ga implantation into crystalline Si annealed at 550–600°C for 30 s. In this case, increasing the anneal temperature to 900°C resulted in a deeper junction due to increased activation and diffusion in the Ga tail region. In the Si preamorphized case, the junction depth is not as dependent on anneal temperature since the Ga channeling tail is substantially reduced (see Fig. 1).

The sheet resistance R_s of the implanted region is seen to generally increase with anneal temperature T_A greater than 550°C. Below 550°C, very little activation takes place resulting in very high R_s [9]. In the neighborhood of 550°C, SPE regrowth of the amorphized layer takes place resulting in activation exceeding the solid solubility limit. For $T_A >$ 550°C, Ga diffusion and precipitation during anneal result in an increasing R_s. Preamorphizing the Si surface layer results in a decrease in R_s upon equivalent Ga implantation. This increase in Ga activation could be due to additional vacancies introduced by the Si preimplant.

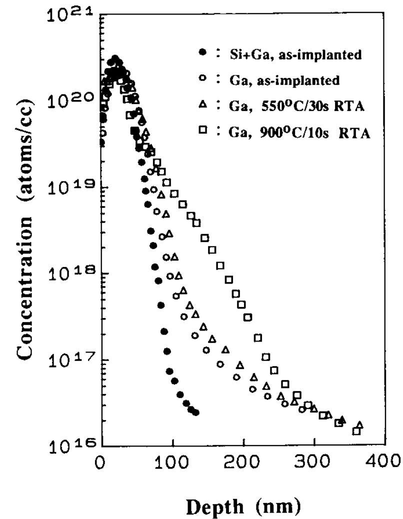

Fig. 1. SIMS profiles of 50-keV Ga-implanted shallow junctions for a dose of $1 \times 10^{15}/cm^2$, including as-implanted RTA-annealed samples at 550 and 900°C.

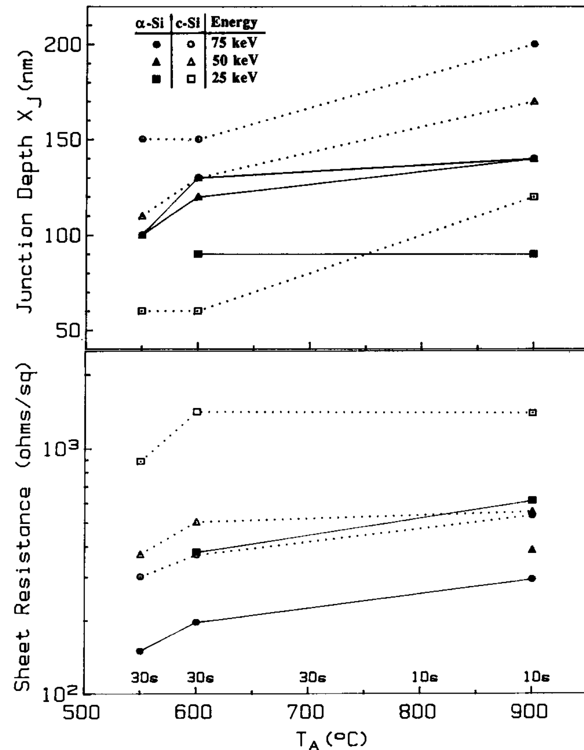

Fig. 2. Junction depths and sheet resistances of 25–75-keV Ga-implanted diodes as a function of annealing temperature. α-Si: surface layer preamorphized by Si self-implant; c-Si: crystalline Si substrate.

$I-V$ characteristics of Ga p^+-n junctions with an area of 900 $\times$ 900 μm^2 implanted at 50 keV with a dose of $1 \times 10^{15}/cm^2$ are shown in Fig. 3. For the non-preamorphized diodes annealed at 600°C, J_R of 1.2 nA/cm^2 at -5 V and an ideality factor of 1.01 (taken from 10^{-8} to 10^{-3} A) were obtained. The

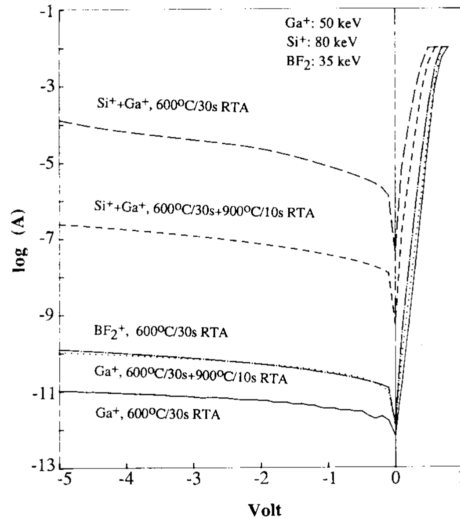

Fig. 3. *I–V* curves of the 50-keV, $1 \times 10^{15}/cm^2$ Ga-implanted diodes, annealed at either 600°C for 30 s or two-step annealed (600°C for 30 s + 900°C for 10 s). The area of the diodes is $900 \times 900\ \mu m^2$. The Si preimplants were performed at 80 keV for a dose of $2 \times 10^{15}/cm^2$. *I–V* curve of 35-keV, $1 \times 10^{15}/cm^2$ BF_2-implanted diode annealed at 600°C for 30 s is also included for comparison.

two-step annealed diodes exhibit larger (10x) leakage current, probably due to precipitation and larger stress effect during the higher temperature (900°C) anneal. For comparison, the *I–V* curve of a diode fabricated by 35-keV BF_2 implantation at the same dose of $1 \times 10^{15}/cm^2$ and annealed at 600°C for 30 s is also shown in Fig. 3. The J_R of these BF_2-implanted diodes is at least one order magnitude higher than the Ga-implanted diodes. This is due to the larger channeling effect of BF_2 implantation which resulted in a broader α–c interface and hence higher J_R. It is interesting to note that the J_R of 45.5-keV BF_2-implanted diodes furnace annealed at 600°C [10] is 10^2 times higher than what we measured for 35-keV BF_2-implanted diodes RTA annealed at the same temperature.

A summary of J_R values (at 5-V reverse bias) for diodes fabricated under various conditions is shown in Table I. The diodes with Si preimplant show a much higher J_R, probably because the damage cannot be completely annealed even up to 900°C. Since a portion of the damage layer resides within the space-charge region as the diodes are reverse biased, it can contribute significantly to the leakage current. This damage layer has been identified in the RBS spectra [6] and was also detected by DLTS measurements where three deep levels have been observed for these Si preamorphized diodes. A lower energy Si preimplant would locate the damage within the p^+ region of the diode with an amorphous layer thinner than the Ga implantation range. However, this thin amorphous layer can no longer effectively eliminate the implantation tail and hence loses the advantage of using Si preimplantation.

To determine the contribution of diffusion and generation currents to the overall leakage, the J_R for the Ga-implanted diode annealed at 600°C was measured over the 10–125°C temperature range. As shown in Fig. 4, the generation current component dominated only up to 70°C. This compares favorably with 30-keV B-implanted diodes annealed at 1000°C which have been reported [11] to have generation current domination up to 110°C.

In summary, Ga-implanted diodes with a junction depth as shallow as 60 nm have been obtained by low-temperature rapid thermal annealing. In our investigation, an optimum trade-off region of required diode properties was obtained with 50-keV Ga implantation annealed at 550–600°C for 30 s, namely junction depth of 100–130 nm, R_s of 375–500 Ω, J_R of 1–1.5 nA/cm², and ideality factor of 1.01–1.03. This Ga-based, low-temperature process appears to produce the neces-

TABLE I
ELECTRICAL PROPERTIES OF 25–75-keV Ga-IMPLANTED DIODES FOR A DOSE OF $1 \times 10^{15}/cm^2$, WITH AND WITHOUT Si PREIMPLANT
All Si preimplants were performed at 80 keV for $2 \times 10^{15}/cm^2$. J_R of 35-keV BF_2-implanted diodes is also included for comparison.

Species	Implant Energy	Anneal Temp / Time	J_R (-5V) (nA/cm^2)
Ga	25 keV	600 C/30s	1.76
	50 keV		1.23
	75 keV		2.9
Ga	50 keV	900 C/10s	12.34
Si+Ga	25 keV	600 C/30s	$1.76X10^7$
	50 keV		$4.5X10^6$
	75 keV		$1.8X10^6$
Si+Ga	50 keV	900 C/10s	$4X10^4$
BF_2	35 keV	600 C/30s	20
BF_2 *	45.5 keV $5X10^{14}/cm^2$	600 C/30 min	2000
Si+BF_2 *	45.5 keV $5X10^{14}/cm^2$	600 C/30 min	$3X10^7$

* data were taken from Ref. 9

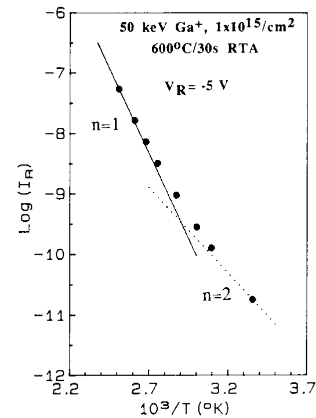

Fig. 4. Arrhenius plot for reverse-bias leakage current of 50-keV Ga-implanted diode RTA annealed at 600°C for 30 s.

sary p^+-n diodes characteristics required for submicrometer PMOS/CMOS technology.

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