Si p^+-n shallow junction fabrication using on-axis Ga$^+$ implantation

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p^+-n shallow junction fabrication using on-axis Ga implantation into crystalline and preamorphized Si, in conjuction with rapid thermal annealing, is reported. The implants are performed at energies of 50 and 75 keV for doses of 1 and $3.5\times10^{15}/\text{cm}^2$. Taking advantage of the short Ga projection range, low critical dosage ($2\times10^{14}/\text{cm}^2$) needed for amorphizing the implanted layer, and a low anneal temperature (550–600 °C) required to induce solid phase epitaxial regrowth and activate the Ga dopants in excess of its maximum solid solubility in Si, a shallow junction at a depth of 100 nm and with sheet resistance of 150 Ω/□ was obtained using 75 keV Ga implantation at a dose of $1\times10^{15}/\text{cm}^2$. The sheet resistance of the Ga-implanted layer can be optimized by adjusting the anneal temperature and time.

In very large scale integration technology, especially for complementary metal-oxide-semiconductor integrated circuits, highly conductive shallow junctions are required for small device fabrication in order to achieve higher packing density and faster switching speed. Shallow n^+-p junctions are normally achieved by implanting heavy donor ions, such as As and Sb, because of their smaller projection ranges (R_p). For p^+-n shallow junctions, the use of B has continued in spite of its long R_p because of its higher solid solubility in Si and smaller diffusivity in SiO_2 than those of heavy acceptor ions, such as Ga and In. However, impractically low-energy implants (<10 keV) and the channeling effect counter the advantages of boron over the heavy ions when a junction depth less than 200 nm is required. Instead of using ^{11}B, $^{49}BF_2$ has been used to allow higher energy implantation and to reduce the channeling effect.[1] The problems, however, have only been partially resolved, since the channeling tail of the BF_2 implant is still quite sizable when compared to ^{69}Ga implants. In addition, the implanted fluorine ions may generate damage[2] which cannot be annealed completely, even at temperature beyond 1000 °C. On the contrary, the channeling effect of Ga implantation is greatly reduced because an amorphous layer is more easily rendered, at a dose of $2\times10^{14}/\text{cm}^2$. The amorphous layer can be solid phase epitaxially regrown by annealing in a low-temperature regime of 550–600 °C, resulting in a highly activated thin layer in which the free-carrier concentration exceeds the maximum solid solubility of Ga in Si.[3,4] Consequently, a good opportunity exists for using Ga implantation to resolve the problems encountered in shallow junction fabrication using B and/or BF_2 ion implantations. The problem with Ga diffusivity in SiO_2 can be eliminated by using photoresist as the mask layer or focused ion beam (FIB) resistless/maskless ion implantation.[5]

In this letter, we report on shallow p^+-n junction fabrication using Ga implantation into crystalline Si and amorphized Si rendered by Si preimplant. Generally, for shallow junction fabrication, 7° off-axis implantation is performed to reduce the channeling effect. However, it has recently been reported that for submicron device fabrication, off-axis implantation results in a shadowing effect which causes asymmetric device characteristics and degrades performance.[6,7] Therefore, in this investigation, all the Ga implantations were performed on-axis. Rapid thermal annealing (RTA) was used to activate the implanted ions while minimizing diffusion.

(100) oriented Si wafers with a 3 μm P-doped (1 Ω cm) epilayer on a Sb-doped n^+ (0.01 Ω cm) substrate were used. First, an 8 nm SiO_2 layer was thermally grown on all wafers, and half of these wafers were ^{28}Si preimplanted, at an implant energy of 80 keV and a dose of $2\times10^{15}/\text{cm}^2$, to form an 160 nm amorphous layer on the surface of the Si substrate.[8] ^{69}Ga implants were then performed at energies of 50 and 75 keV, and two different doses of 1×10^{15} and $3.5\times10^{15}/\text{cm}^2$. The implants were implemented at a current density less than 0.8 $\mu\text{A/cm}^2$ to avoid ion beam annealing during implantation. All the wafers were subsequently heat treated by rapid thermal annealing (RTA) using an A. G. Associates Heatpulse 410 system at annealing temperatures between 550 and 1000 °C for 10–90 s. The Ga-implanted atomic concentration profiles before and after RTA treatment were characterized by secondary ion mass spectrometry (SIMS) using the Cameca IMS-3*f* system with a 10.5 keV O_2^+ ion beam. A comparison between as-implanted gallium SIMS profiles with and without Si preimplant is shown in Fig. 1(a) at a dose of $1\times10^{15}/\text{cm}^2$ for both 50 and 75 keV Ga implants. Channeling tails, because of the on-axis implant, are present in the Ga-implanted samples without Si preimplant, but much reduced in the samples with Si preimplant. The SIMS profiles of Ga-implanted samples (with and without Si preimplant), after RTA treatments at 600 °C for 30 s or 900 °C for 10 s, are plotted in Fig. 1(b). In samples RTA annealed at 600 °C for 30 s, with and without Si preimplant, there is no perceptible movement of the Ga SIMS profiles from the as-implanted samples. The sheet resistance and junction depth of the Ga-implanted thin layers, which can be obtained from four-point probe (FPP) and spreading resistance profiling (SRP) measurements,[9] are 200 Ω/□ and 120 nm for the sample with Si preimplant, and 370 Ω/□ and 150 nm for the sample without Si preimplant. Lower sheet resis-

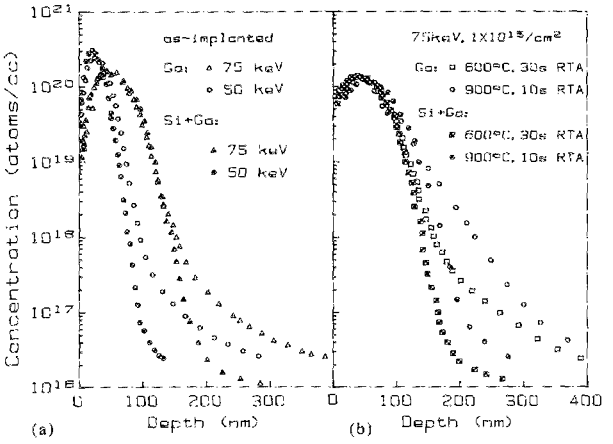

FIG. 1. SIMS profiles of Ga-implanted samples at 50 and 75 keV with a dose of 1×10^{15}/cm^2. (a) As-implanted samples and (b) 75 keV Ga-implanted samples, preamorphized and nonpreamorphized, after RTA at 600 and 900 °C.

tance is generally obtained for samples with Si preimplant for which the Ga activation was enhanced. After RTA treatment at 900 °C for 10 s, Ga diffused into Si, resulting in deeper junctions. This was especially pronounced for the sample without Si preimplant where the diffusion of the channeling tail was enhanced, as shown in Fig. 1(b). Junction depths of 140 and 200 nm and sheet resistances of 295 and 535 Ω/□ are obtained after RTA for the samples with and without Si preimplant, correspondingly. As reported by Harrison *et al.*,[3] these larger sheet resistances are due to the precipitation of Ga ions in Si at the higher temperature anneal.

Rutherford backscattering spectrometry (RBS) in the channeling mode was performed with a 2 MeV He$^+$ ion beam. From the aligned spectra of the as-implanted samples shown in Figs. 2(a) and 2(b), amorphous layers of 175 and 120 nm are measured to have been produced by the Ga implantation, with and without Si preimplant, respectively. The amorphous layers of both samples with and without Si preimplant were regrown by RTA at 600 °C for 30 s, and the activated Ga percentage is estimated to be about 75%, after anneal. As compared to the sample with Si preimplant, a higher backscattering peak shown in the Si surface of the sample without Si preimplant implies that the regrowth was less complete. This is consistent with the higher sheet resistance for the samples without preimplant as compared to the preamorphized samples. However, as shown in Fig. 2(a), an end-of-range damage region due to the Si preimplant is not fully annealed, leading to another backscattering peak in the aligned spectrum. RBS in channeling mode was also performed for the Ga-implanted samples annealed at 900 °C for 10 s. Compared to the aligned spectra of samples annealed at 600 °C, although the damage of the implanted layer is reduced, a higher Ga backscattering peak was observed for the 900 °C RTA, which confirmed the occurrence of the Ga precipitation in Si.

Figure 3 shows the sheet resistance of samples implanted with 75 keV Ga at a dose of 1×10^{15}/cm^2 (with and without Si preimplant) as a function of annealing temperature. Generally, the sheet resistance of the samples with Si preimplant is lower than those of the samples without Si preimplant. The lowest sheet resistance obtained is 150 Ω/□ for the samples with Si preimplant annealed at 550 °C for 30 s, while the lowest value obtained for the samples without Si preimplant is 220 Ω/□ after annealing at 700 °C for 30 s. Optimization of the sheet resistance by RTA annealing the sample in the 550–600 °C temperature regime was attempted by varying the anneal time from 15 to 90 s. The results, shown in the inset to Fig. 3, reveal no significant difference in sheet resistance with annealing time. This implies that the amorphous layers can be regrown, and the implanted Ga ions can be highly activated, with a low-temperature anneal in a short period of time of less than 15 s.

For B- and BF$_2$-implanted samples, lower sheet resistance is usually achieved by activating the impurities at higher annealing temperature, which in turn results in a deeper junction. Therefore, in practice, a trade-off between sheet resistance and junction depth is necessary. An example of a 49 keV BF$_2$ implant at 7° off-axis reported by Wu *et al.*[1] is plotted in Fig. 4. At annealing temperatures of 550–600 °C,

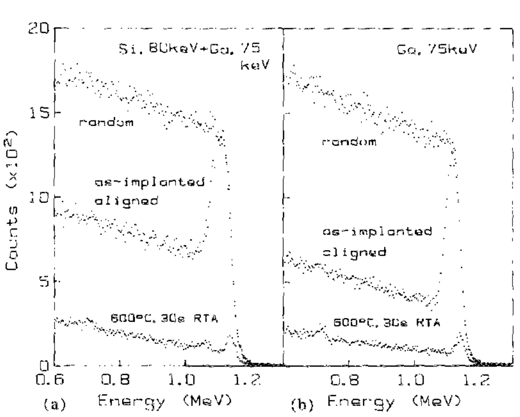

FIG. 2. RBS/channeling random and aligned spectra for on-axis Ga-implanted samples, at the energy and dose of 75 keV and 1×10^{15}/cm^2. (a) Preamorphized sample before and after 600 °C, 30 s RTA and (b) nonpreamorphized sample before and after 600 °C, 30 s RTA.

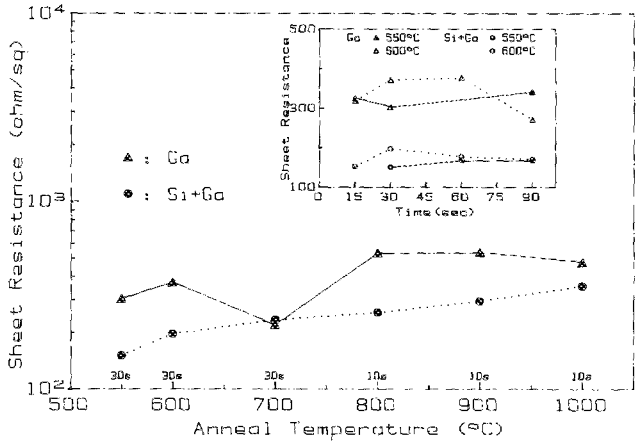

FIG. 3. Sheet resistance of the Ga-implanted samples vs RTA anneal temperature. The implant energy and dose are 75 keV and 1×10^{15}/cm^2, respectively. The inset shows the sheet resistance of the Ga-implanted samples annealed at 550 and 600 °C as a function of annealing time.

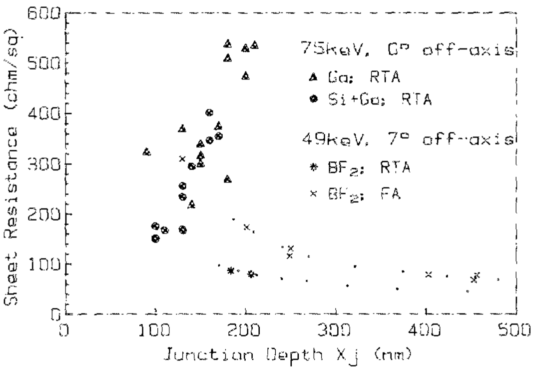

FIG. 4. Sheet resistance vs junction depth for the 75 keV on-axis Ga-implanted sample at a dose of $1\times10^{15}/\text{cm}^2$ after RTA treatment at various temperatures. The data for the 49 keV, 7° off-axis BF$_2$ implantation at a dose of $2\times10^{15}/\text{cm}^2$ (see Ref. 1) are included for comparison.

although the junction depth is reduced to less than 150 nm, the sheet resistance increased substantially, to above 300 Ω/□. By comparison, Ga-implanted samples exhibit a different relationship between sheet resistance and junction depth. In this case, by decreasing the annealing temperature to the range of 550–600 °C, not only can one obtain a shallow junction since no thermal diffusion will occur, but also a low sheet resistance can be achieved because of the implanted Ga ions being highly activated through the solid phase epitaxial regrowth of the implanted amorphous layer. For the 75 keV Ga-implanted samples at the dose of $1\times10^{15}/\text{cm}^2$, also shown in Fig. 4, one can obtain both a shallow junction depth of 100 nm and a low sheet resistance of 150 Ω/□ for the sample with Si preimplant annealed at 550 °C for 30 s.

In summary, shallow junction fabrication by on-axis Ga implantation into crystalline and preamorphized Si has been investigated. Unlike boron, which requires high temperature to obtain high activation percentage, to activate the implanted Ga impurities only a low-temperature annealing in the 550–600 °C range for 15 s is necessary. A junction depth of 100 nm with a sheet resistance of 150 Ω/□ was achieved in the 75 keV Ga-implanted sample with Si preimplant. From the Ga SIMS profiles of samples implanted at energies of 50 and 75 keV, the junction depth is observed to be proportionally reduced by reducing the implantation energy. Comparing samples with and without Si preimplant, it has been observed that the sheet resistance is lower and the junction depth is smaller for the samples with Si preimplant since the preimplant eliminates the channeling tail and enhances the dopant activation. However, from the RBS/channeling spectrum of the sample with Si preimplant annealed at 600 °C for 30 s, it has been seen that the end-of-range damage caused by Si preimplant is not completely annealed. This may affect the junction electrical characteristics, such as leakage current and breakdown voltage. The quality of the highly activated shallow Ga-implanted p^+-n junctions is currently under investigation.

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