The Effect of Trench-Gate-Oxide Structure on EPROM Device Operation

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Abstract—**A novel floating-gate erasable programmable read-only memory (EPROM) cell with a trench-gate-oxide (TGO) structure near the drain region was fabricated using electron-beam lithography technology. Several promising advantages were found for the TGO cell. The writing time for the TGO devices was measured to be 100 times faster than for conventional devices of the same dimensions. Two-dimensional (2-D) simulation of the TGO structure indicated that longitudinal and transverse channel electric fields are generated which simultaneously increase the hot-electron population in the channel and the injection efficiency into the floating gate.**

I. INTRODUCTION

THE floating-gate hot-electron injection approach has been widely accepted for erasable programmable read-only memory (EPROM) cells, due to its compatibility with standard MOS processes and high reliability. In conventional EPROM operation, one faces a biasing dilemma to enhance the writing speed through higher injection current [1]. High drain and low gate voltage are required for increasing the hot-electron population in the channel, while the reverse is needed for high injection probability. In this paper we report on a novel device structure, the trench gate oxide (TGO) shown in Fig. 1, which uses a thinner gate oxide for a finite portion of the channel near the drain region. The TGO approach relaxes the bias requirements and substantially increases the writing and erasing efficiency. Device simulation indicates that a combination of high transverse field and channel "hot-" electron generation results in the high injection current of the TGO device.

II. DEVICE FABRICATION

The following devices have been fabricated: a) conventional and TGO-structure MOSFET's with single and coupled floating-gate configuration [2]; and b) conventional and TGO EPROM cells. For device fabrication we have used p-type, (100) Si wafers with a doping density of 1×10^{15} cm^{-3}. The channel implantation dose was 1.5×10^{12} cm^{-2}. The gate length had a design value of 3 μm. The gate oxide trench had a nominal width of 0.4 μm (D_1) and was located 1.0 μm (D_2) away from the drain side of the gate edge. To achieve highly accurate alignment necessary for the TGO structure, direct write e-beam lithography was used. Devices with gate oxide thickness of 300 and 600 Å were fabricated. The trench oxide of 70 Å was obtained by reoxidation after trench definition and etching. The polysilicon gates were obtained by LPCVD deposition at 580°C with *in-situ* phosphorus doping. Both conventional and TGO devices were fabricated within the same chip. For the EPROM devices we have used a self-aligned double poly-Si process. A thermal inter-poly oxide of about 600 Å was used.

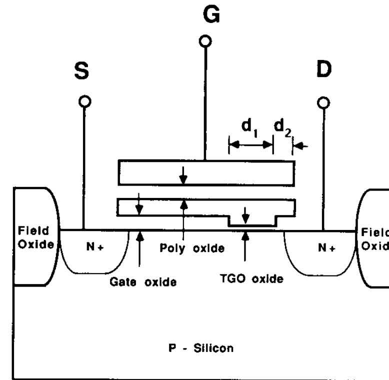

Fig. 1. The TGO memory device structure with the thin gate oxide portion near the drain region.

III. RESULTS AND DISCUSSION

Table I gives representative experimental values of the transconductance g_m and the threshold voltage V_{th} for two conventional MOSFET's (with 300- and 70-Å gate oxides) and the TGO MOSFET with 300-Å gate oxide and 70-Å trench gate oxide. The TGO FET exhibits V_{th} values which fall in between those of the two conventional FET's but a high g_m which approaches that of the conventional device with the thin uniform gate oxide. This is due to the fact that the effective channel length of the TGO device is shorter than the (300-Å gate oxide) conventional device since it is only controlled by the thick oxide region. Operating with the trench near the drain region results in a larger g_m since the stronger transverse field in the trench retards the conduction channel pinch-off. No asymmetry due to implantation shadowing effect was observed when the source and drain were interchanged in the conventional devices. Fig. 2 shows L_d and L_g versus V_g to indicate the injection efficiency with gate bias for both the conventional and TGO MOSFET's. To accurately measure L_g, devices with the coupled floating-gate structure [2] were included in the overall chip. In this structure a single

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TABLE I
COMPARISON OF TRANSCONDUCTANCE AND THRESHOLD VOLTAGE FOR CONVENTIONAL AND TGO MOSFET'S WITH ASPECT RATIO OF 20

Lnom=3µm	Conventional		TGO	
	tox=300Å Leff ~1.6µm	tox=70Å Leff ~1.6µm	tox=300Å , TGO=70Å Lnom=3µm , Leff ~1.1µm trench@drain	trench@source
g_m V_g=4V V_d=5V	1.5 mS	4.6 mS	3.7 mS	3.2 mS
V_{th} V_d=0.1V I_d=1µA	0.89 V	0.51 V	0.69 V	0.70 V

poly-Si floating gate connects two identical transistors, which are used independently for programming and for evaluation of charge on the floating gate through V_{th} measurements. This technique allows the measurement of injected charge on the floating gate independent of possible stress effects. As shown in the insert of Fig. 2, at low gate voltage the injection efficiency for the TGO MOSFET appears lower than the (300-Å) conventional approach, while for V_g larger than 4 V the situation is reversed. At 7-V gate bias the TGO device displays a 100 times increase in injection efficiency. This performance is highly desirable for the memory application since the *read* and *write* operations can take place at very low and very high injection efficiency, respectively.

The two-dimensional (2-D) simulation program BAMBI [3] was used to analyze the TGO device structures. The transverse (vertical) electric field is plotted in Fig. 3(a) along the length of a 1-μm section through the channel. While the conventional device with 600-Å gate oxide exhibits an E-field monotonically decreasing from source to drain, the TGO case shows a sharp increase in E-field at the trench leading edge. Fig. 3(b) shows the surface potential of channel electrons under various conditions. The four lower curves are for a V_g of 2.5 V, while the upper curve is for 6 V. The increase in electron potential due to the trench is more pronounced with decreasing trench oxide thickness. For the case of the 70-Å trench oxide and V_g of 6 V, there is a sharp step increase in electron potential at the trench edge, sufficient (3.2 eV) for electrons to overcome the oxide potential barrier [4]. In this case, the channel electrons become "hot" within a short distance of the trench edge. With the assistance of the strong oxide field at the same location, a higher injection probability is combined with a higher hot-electron concentration leading therefore to a high injection rate. However, if the gate voltage is lower (say 2.5 V), from Fig. 3 we find the more gentle slope of the potential profile will result in a reduced channel field which in turn reduces the hot-electron generation rate of channel electrons and hence lessens the hot-carrier population. This is a possible explanation for the experimental observation that at high V_g the injection efficiency of the TGO device is higher than the conventional device, whereas the reverse is the case at low V_g.

Experimental results on programming the TGO EPROM are compared with conventional operation in Fig. 4. The TGO cell displays a writing speed enhancement of 100 over a wide frequency range. The writing speed enhancement is consistent

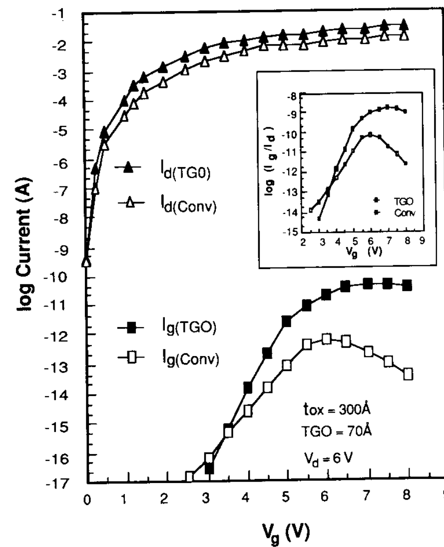

Fig. 2. Comparison of gate and drain currents for the TGO and conventional EPROM cell versus the gate voltage. The TGO device has a 0.4-μm (d_1) trench width located 1 μm (d_2) away from the drain-side gate edge. The conventional gate oxide is about 300 Å.

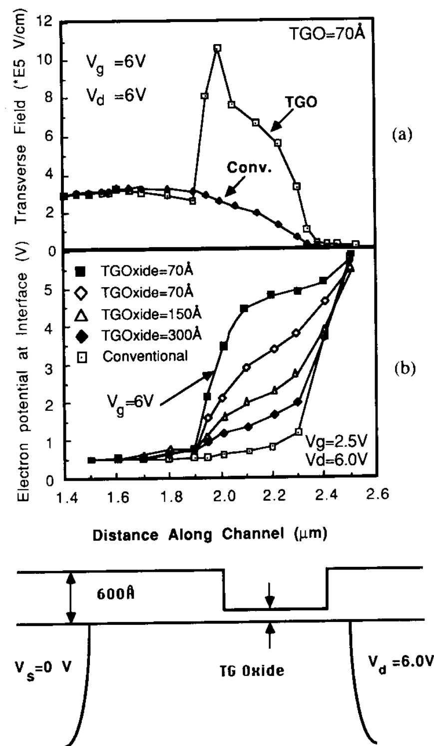

Fig. 3. BAMBI simulation results for channel electrons: (a) transverse electric field; and (b) the electron surface potential energy for different TGO thickness and bias conditions. The conventional gate oxide is 600 Å.

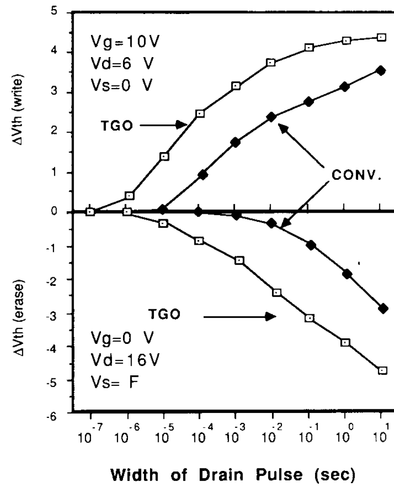

Fig. 4. Comparison of the writing and electrical erasing characteristics of the TGO and conventional memory devices. The conventional gate oxide and TGO are about 300 and 70 Å, respectively.

with the higher injection rate observed in the TGO MOSFET. The electrical erase operation is made possible in this device by applying high drain voltage (> 16 V), but grounding the gate and floating the source as in the erasing mode of the FLOTOX memory cell [5]. Fig. 4 shows the promising potential of the TGO EPROM for the flash memory application [6].

IV. Summary

EPROM devices have been fabricated with thin trench gate (70 Å) oxide near the drain region. Several promising features were found for the TGO MOSFET and EPROM: 1) high transconductance; 2) fast programming; 3) good tolerance to unintentional writing during the readout operation; 4) showing potential for flash erase application.

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